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30-GHz MONOLITHIC RECEIVE MODULE

**Interim Report for Period
November 1, 1985–October 31, 1987**

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16. Abstract This report describes the fourth year progress on a program to develop a 27.5 to 30-GHz GaAs monolithic receive module for spaceborne-communication antenna feed array applications, and to deliver submodules for experimental evaluation. Program goals include an overall receive module noise figure of 5 dB, a 30 dB RF to IF gain with six levels of intermediate gain control, a five bit phase shifter, and a maximum power consumption of 250 mW. Submicron gate length single and dual gate FETs are described and applied in the development of monolithic gain control amplifiers and low noise amplifiers. A two-stage monolithic gain control amplifier based on ion implanted dual gate MESFETs was designed and fabricated. The gain control amplifier has a gain of 12 dB at 29 GHz with a gain control range of over 13 dB. A two-stage monolithic low noise amplifier based on ion implanted MESFETs which provides 7 dB gain with 6.2 dB noise figure at 29 GHz was also developed. An interconnected receive module containing LNA, gain control, and phase shifter submodules was built using the LNA and gain control ICs as well as a monolithic phase shifter developed previously under this program. The design, fabrication, and evaluation of this interconnected receiver is presented. Progress in the development of an RF/IF submodule containing a unique ion implanted (continued)			
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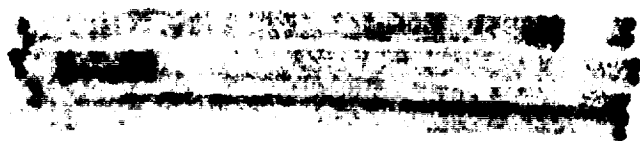
16. Abstract (Continued)

diode mixer diode and a broadband balanced mixer monolithic IC with on-chip IF amplifier and the initial design of circuits for the RF portion of a two submodule receiver are also discussed.

17. Key Words (Continued)

30/20 Communications Satellite
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Monolithic Mixer
Dual Gate FETs
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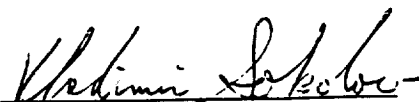
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I. SUMMARY

This report covers the progress made during the fourth and fifth years of a program to develop a 30 GHz monolithic receive module for communication antenna feed array applications, and to deliver submodules and 30 GHz monolithic receive modules for experimental evaluation. Key requirements include an overall receive module noise figure of 5 dB, a 30 dB RF-to-IF gain with six levels of intermediate gain control, a 5 bit phase shifter, and a maximum power consumption of 250 mW. In addition, the monolithic receive module design addresses a cost goal of less than \$1,000 (1980 dollars) per receive module in unit buys of 5,000 or more, and a mechanical configuration that is applicable to a space-borne phased array system. These requirements are summarized as performance goals in Table S-1.

A baseline design of the monolithic module was accomplished during the first year in Task I. The design includes partitioning of the receiver into four submodule functions: low noise amplification (LNA), digital phase control (PS), gain control (GC) and RF/IF frequency down-conversion, as shown in Figures S-1 and S-2. The PS, GC, RF/IF and LNA functions embodied in the monolithic receive module are developed as individual submodules, each fabricated on a separate chip (Tasks II-V respectively), and designed to permit their interconnection to form the interconnected receive module (Task VI).

In 1986, an initiative was begun to further integrate the receiver by partitioning the receiver into two submodules:

- o A receiver submodule containing the LNA, phase shifter, and gain control amplifier on a single IC
- o An RF/IF submodule containing the mixer, IF amplifier, and LO buffer amplifier

TABLE S-1. NASA'S KEY PERFORMANCE GOALS

Design Parameter	Performance Goal
RF Band	27.5 - 30 GHz
IF Center Frequency	Between 4 - 8 GHz
Noise Figure at Room Temperature	≤ 5 dB
RF/IF Gain	< 30 dB at highest level of gain control
Gain Control	At least six levels: 30, 27, 24, 20, 17 dB and Off
Phase Control	5 bits, each bit $\pm 3^\circ$ at band center
Module Power Consumption	250 mW in all states. In OFF state, 25 mW
Phase and Gain Control	Operate on digital input
Mechanical Design	Fully monolithic construction, compatible with 30 GHz spaceborne phased array applications
Unit Cost	Less than \$1000 (1980 dollars) in unit buys of 5000 or more

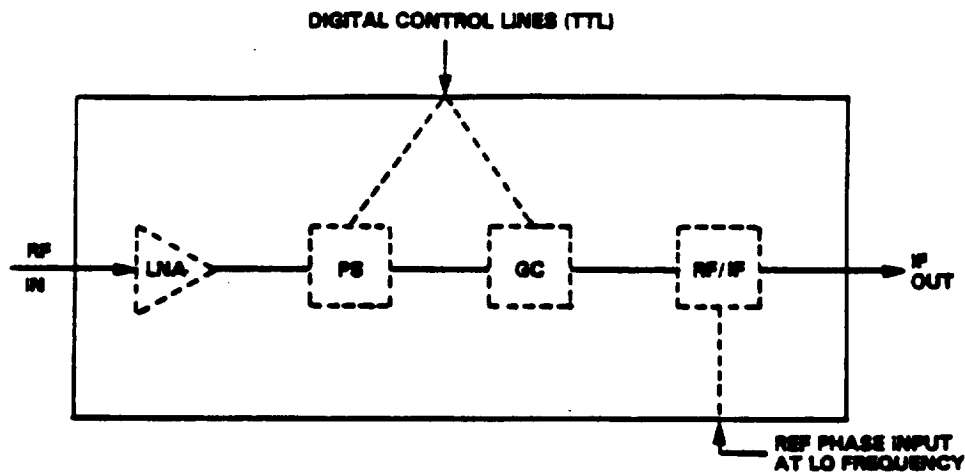


Figure S-1. Submodule Functions of Receive Module

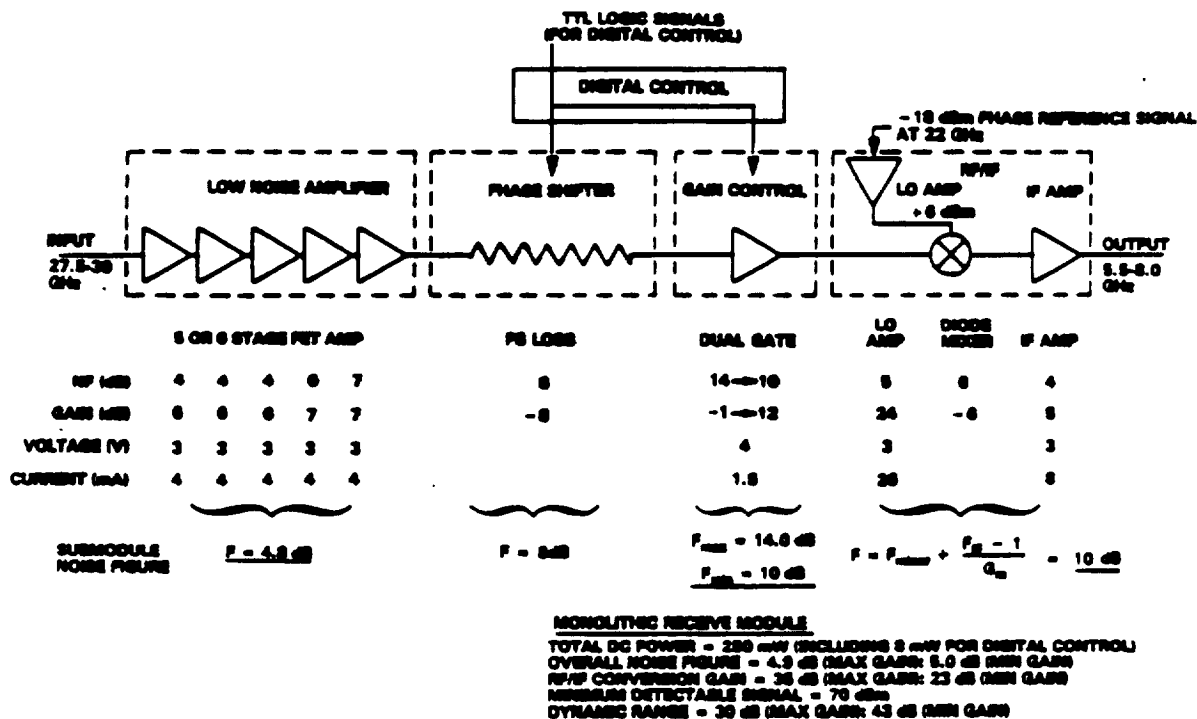


Figure S-2. Block Diagram of Overall Monolithic Receiver

This receiver, composed of two ICs, is called the Cascaded Two Submodule (CTS) receiver. The development of the receiver submodule will be done under a continuation of Task VII.

During 1986 and 1987, work concentrated on the following areas:

- o Development of monolithic LNA and gain control amplifiers for the receiver submodule
- o Development of the mixer IF amplifier, and LO buffer amplifier for the RF/IF submodule
- o Design and fabrication of an interconnected receiver containing the LNA, gain control amplifier and phase shifter
- o Initial design of a phase shifter and two, four, and six stage LNAs for the CTS receiver

Key accomplishments were:

- o Demonstration of a two-stage monolithic gain control amplifier using dual gate FETs with 12 dB gain at center band and a gain control range of over 13 dB
- o Delivery of 100 gain control amplifiers
- o Demonstration of a two-stage LNA with 7dB gain and 6.2 dB noise figure - 10 LNAs were delivered
- o Development of a modified mixer design for 300 ohm diode resistance and demonstration of the 22 GHz LO buffer amplifier
- o Development and demonstration of an interconnected receiver containing the LNA, phase shifter, and gain control amplifier - one interconnected receiver was delivered.
- o Design and fabrication of the first iteration CTS receiver mask set and demonstration of a new reduced size phase shifter design with on-chip logic.

A summary of these accomplishments follows below.

In 1985 we discovered a design deficiency in the dual gate FET that caused RF instability. The design was modified to eliminate this problem and a two stage amplifier design was developed and fabricated using the new dual gate FET design. The first run of these amplifiers gave promising results but on-chip modifications were required to bring the operating frequency of the

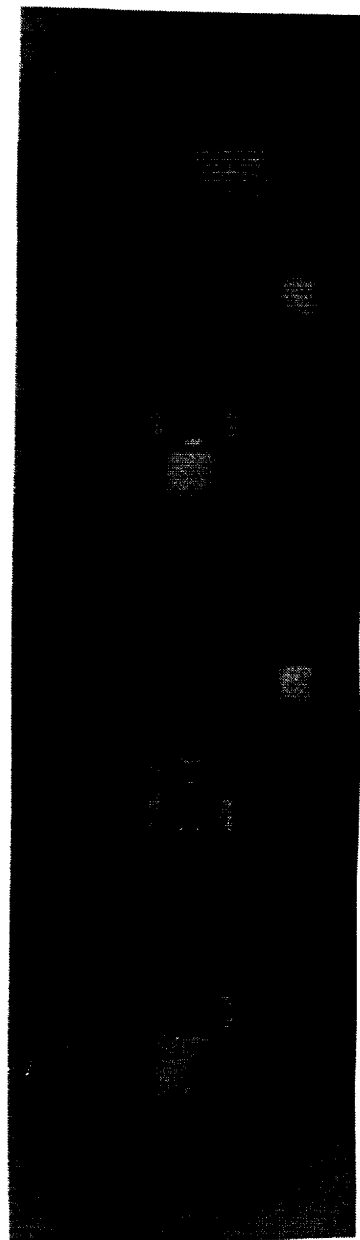
amplifier into the 27.5 - 30 GHz band. A partial delivery of 47 gain control ICs was made from this first run. The knowledge gained from evaluating these amplifiers was used to generate a modified design. ICs based on this design were successfully demonstrated and used for the gain control amplifiers in the integrated receiver. The completed amplifier chip shown in Figure S-3, measures $1.83 \times 0.51 \times 0.15 \text{ mm}^3$. The remaining gain control amplifier chips were delivered from this run to complete the delivery of 100 gain control amplifiers.

Two stage LNAs were fabricated on the same wafers as the gain control amplifiers. A two stage LNA with 7 dB gain and 6.2 dB noise figure was demonstrated in 1986. Ten LNA chips were delivered to NASA to complete the LNA delivery. The LNA ICs were also used to construct the integrated receiver. The completed LNA chip, shown in Figure S-4, measures $2.3 \times .71 \times 0.15 \text{ mm}^3$.

The RF/IF IC containing the mixer and IF amplifier is under development. In 1986 we completed the mixer and IF amplifier designs and began fabrication of the IC. The RF/IF IC will be completed in 1987.

A preliminary integrated receiver containing all RF functions (LNA, gain control, and phase shifter) was designed and fabricated at Honeywell and demonstrated at NASA Lewis in 1986. The completed receiver is shown in Figure S-5. Operation of gain and phase shift control was demonstrated over the 27.5 - 30 GHz band. The noise figure of the completed receiver was 14 dB at the highest gain setting. The high noise figure is due to insufficient preamplifier gain in the two stage LNA, and high noise figure of the following phase shifter and gain control circuits. In 1987 we began fabrication of 4 and 6 stage LNA designs to provide higher front end gain. We anticipate that the six-stage amplifier being developed for the CTS receiver will provide a gain of 30 dB which will reduce the receiver noise figure to an acceptable level (~5 dB).

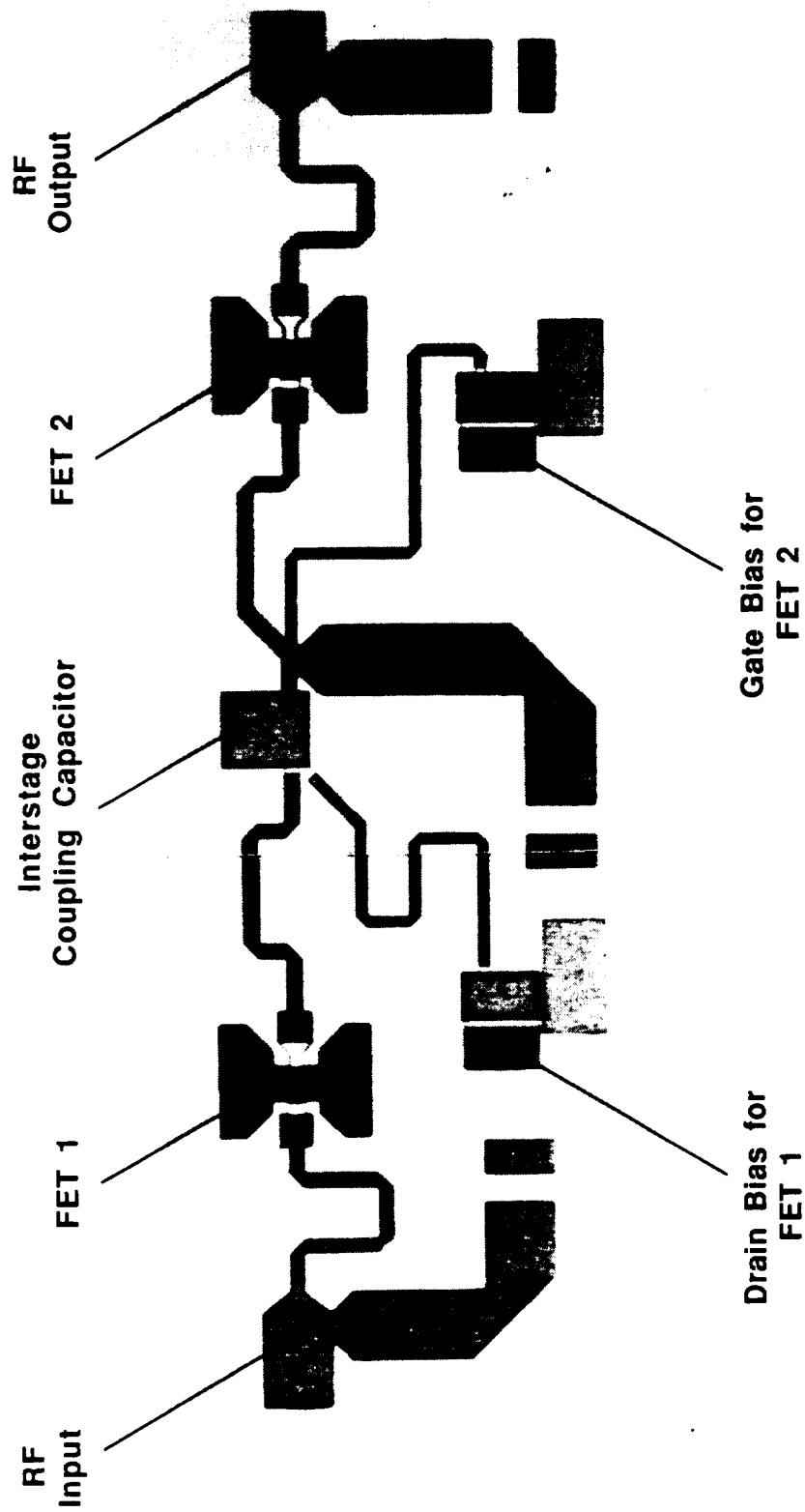
"Design Alternatives"



INPUT

OUTPUT

Figure S-3. Final Design Two-Stage Gain Control Amplifier IC.



Chip Dimensions $2.3 \times 0.71 \times 0.15 \text{ mm}^3$

Figure S-4. Two-Stage Low Noise Amplifier.

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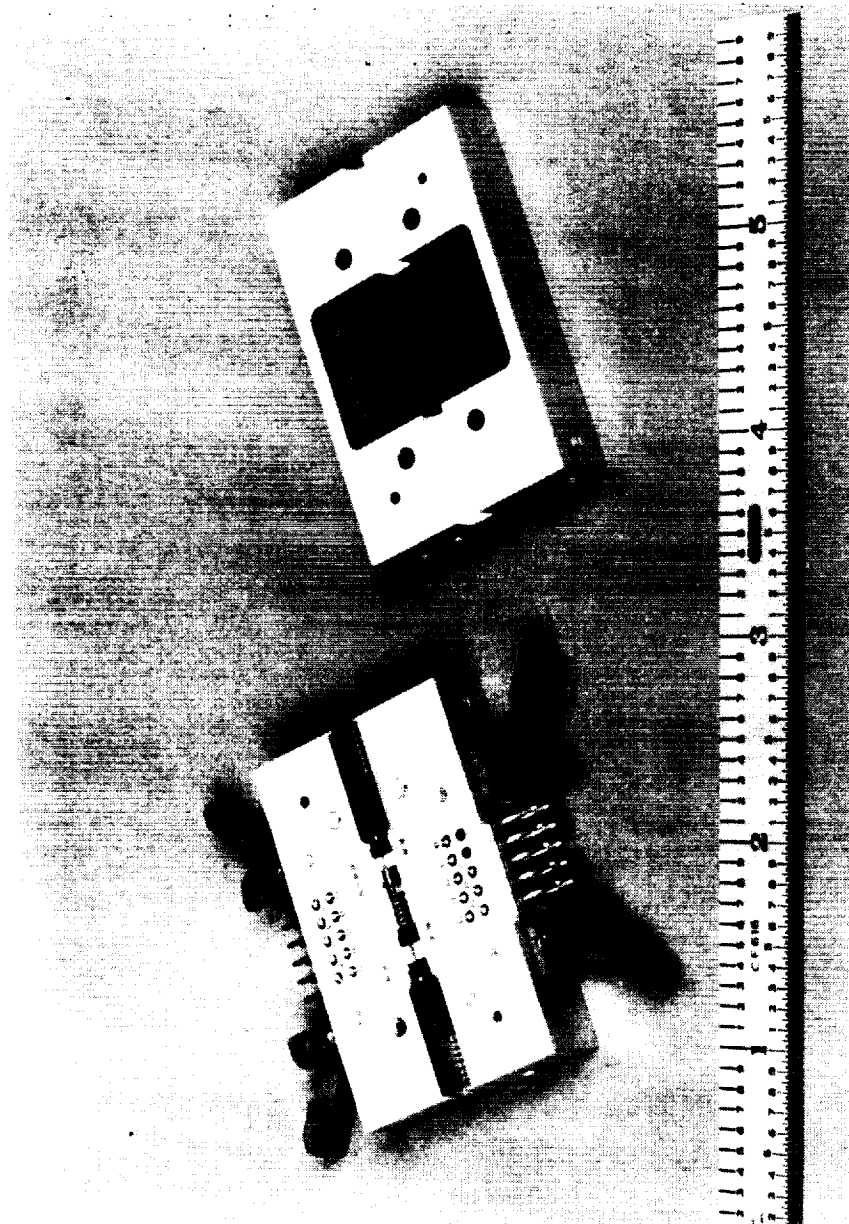


Figure S-5. Three Chip Receiver Assembled in Single Housing with Cover Removed.

II. PROGRAM PROGRESS BY TASKS

The objective of the program is to develop a 30GHz monolithic receive module for communication antenna feed array applications, and to deliver submodules and 30GHz monolithic receive modules for experimental evaluation.

Since Tasks 1 and 2 are completed and have been reported in earlier annual reports, the present report will refer to tasks III through X exclusively.

1.0 GAIN CONTROL AND LNA FABRICATION AND EVALUATION - TASKS III AND V

This section reports on Tasks III and V, the gain control amplifier and low noise amplifier submodule developments. The objectives of these tasks are as follows:

- o Gain Control Amplifier (GCA) - The GCA submodule must provide five levels of RF-to-IF gain (30, 27, 24, 20 and 17 dB) and an off state. The worst case noise figure for the gain control submodule should be less than 14 dB.
- o Low Noise Amplifier (LNA) - The LNA submodule must provide again of 32 dB with a noise figure no worse than 4.8 dB over the 27.5 - 30 GHz frequency range.

The LNA submodule gain and noise figure requirements translate into a requirement for 6 dB gain with 4 dB noise figure for a single amplifier stage. Critical achievements related to the gain control and LNA include:

- o Demonstration of a new dual gate FET design with improved stability
- o Demonstration of 1 and 2-stage gain control amplifiers
- o Demonstration of a 2 stage LNA with 7 dB gain and 6.2 dB noise figure
- o Delivery of 100 gain control amplifier ICs completing Task III
- o Delivery of 10 low noise amplifiers completing task V

These accomplishments are described in the following sections.

1.1 Design and Fabrication of Dual Gate FET for Gain Control Amplifier

As we reported in the third annual report, evaluation of the first gain control amplifier design uncovered an instability problem associated with the layout of the dual gate FET. This led to a redesign of the dual gate FET to eliminate feedback caused by use of a single grounding pad for the FET source and the on-chip RF bypass capacitor connected to the second gate (gain control terminal) of the FET. In 1986 a number of wafers were completed containing the new dual gate FET design. A photomicrograph of the completed device is shown in Figure 1. Typical device drain I-Vs are shown in Figure 2. This new device layout did eliminate the RF instability problems as we predicted.

1.2 One and Two-Stage Gain Control Amplifier Designs

One and two-stage gain control amplifiers were designed using an equivalent circuit model of the dual gate FET based on a cascode connection of single gate FETs. Initially values for the elements in the model were taken from equivalent circuit models of single gate FETs. These element values were used to design the second iteration one and two-stage amplifiers. In 1986 we updated this equivalent circuit model based on S-parameter measurements made with our 8510 network analyzer. The S-parameters were measured for a single discrete dual gate FET, including the on-chip capacitor, in the frequency range 2-26 GHz. To ensure adequate bypass at lower frequencies, an external 47 pF capacitor was connected from the second gate (in parallel with the on chip 1.7 pF capacitor) to ground. The equivalent circuit element values were adjusted using EESOF's Touchstone optimization program to fit the calculated S parameters to the measured data over the 2-26 GHz band. This resulted in the equivalent circuit shown in Figure 3. This updated equivalent circuit was used to develop the third iteration two-stage gain control amplifier design.

The single stage amplifier circuit diagram is shown in Figure 4. The input and output impedance matching networks are realized with sections of high impedance (90-100 ohms) microstrip transmission lines and silicon nitride MIM capacitors. Since the output resistance of a dual-gate FET is significantly increased over its single-gate counterpart ($R_{out} \sim R_{ds1} \times R_{ds2} \text{ gm}^2$ at low frequencies), impedance matching at the output requires high transformation

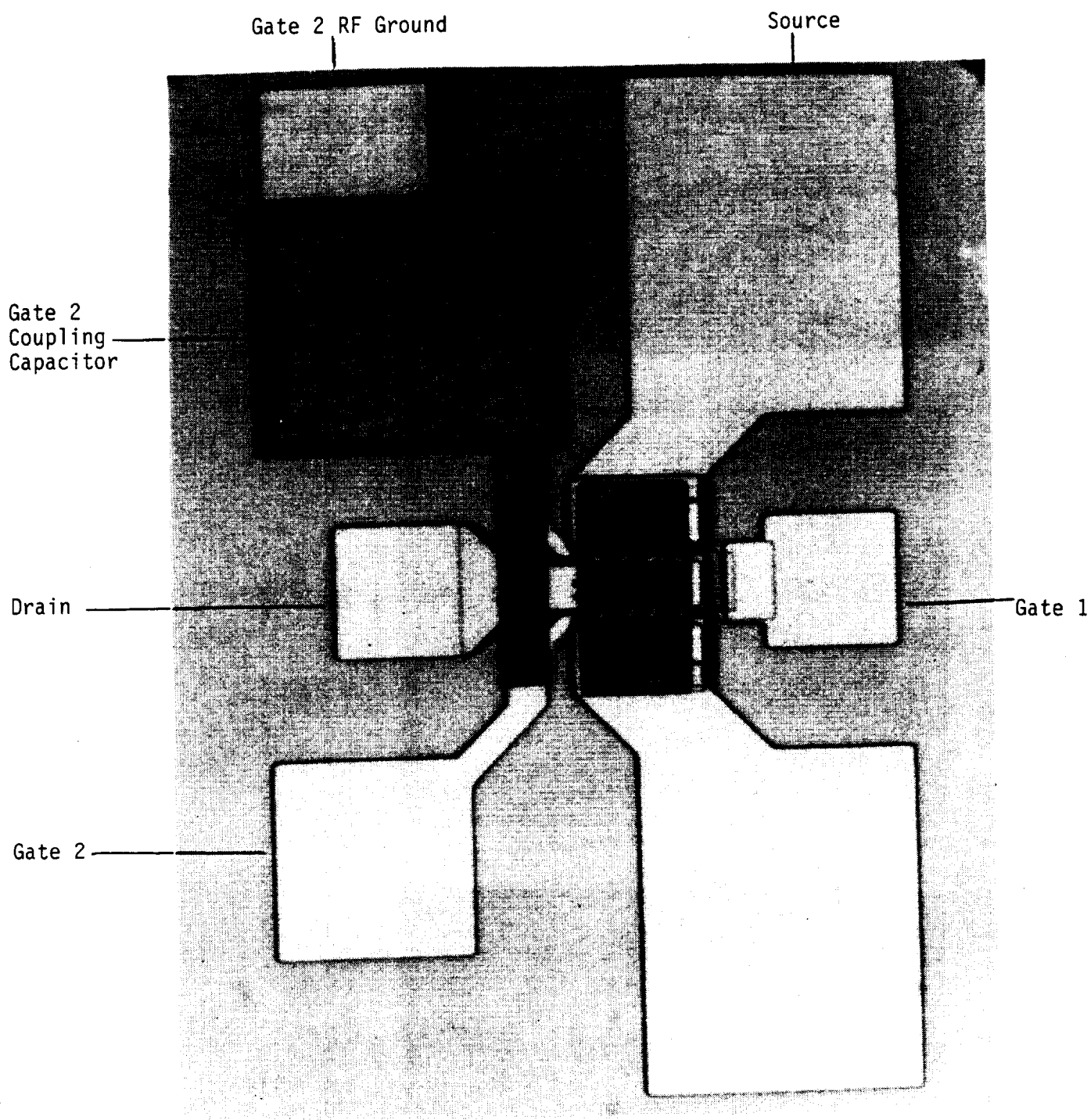
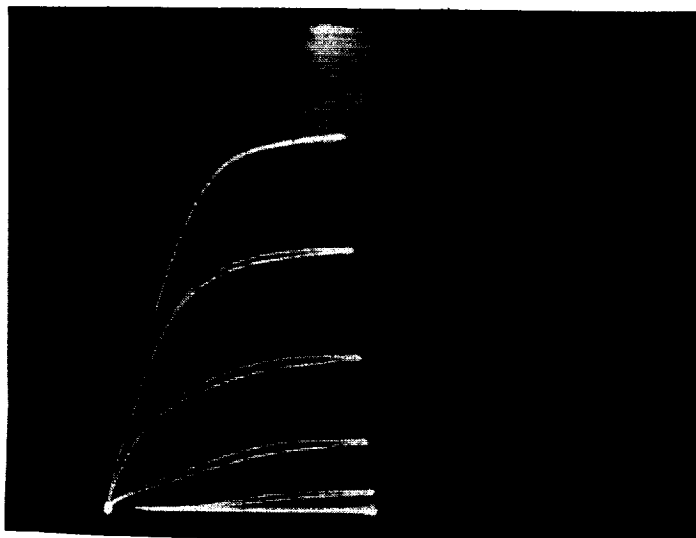
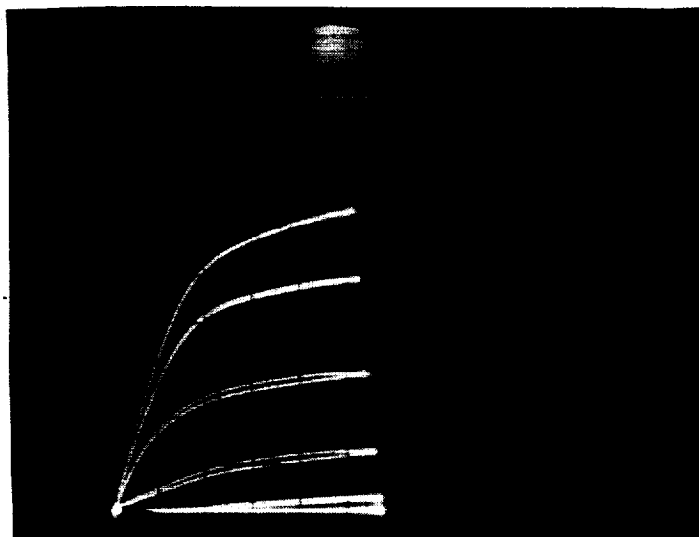


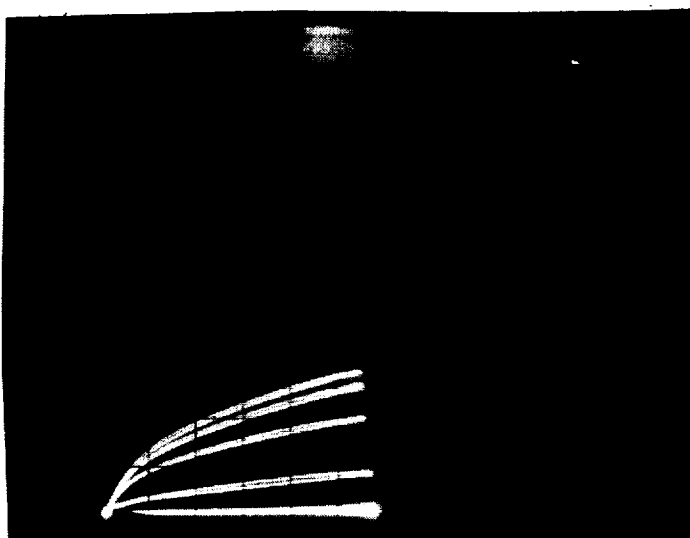
Figure 1. New Dual Gate FET.



$V_{g2} = +.58V$
 2ma/div - vertical
 .5V/div - horizontal
 .5V/step

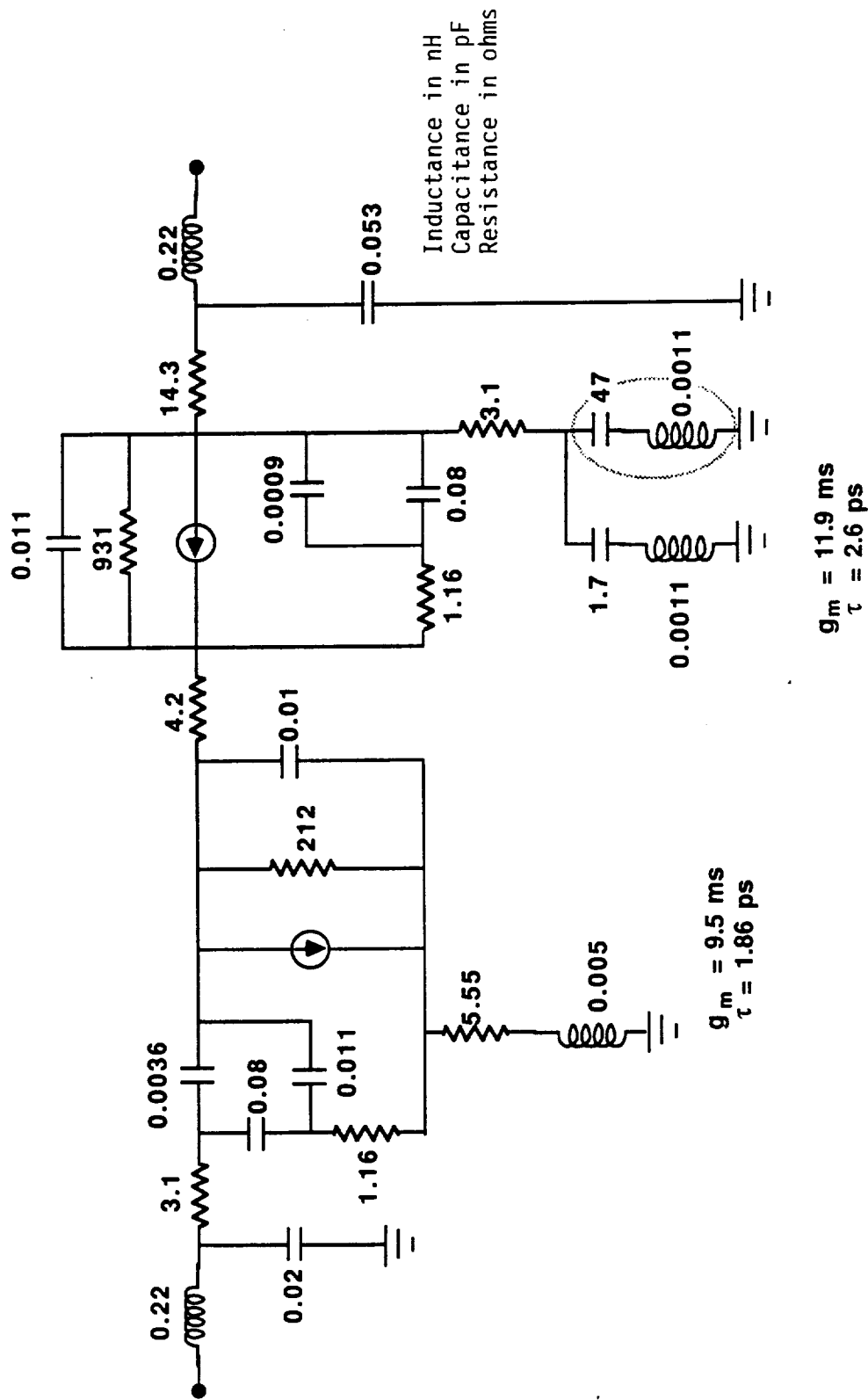


$V_{g2} = 0V$



$V_{g2} = -1V$

Figure 2. DC Drain IVs of .25 x 100 Micron Dual Gate FETs.



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Figure 3. Equivalent Circuit Derived from Measured S-Parameters for 2x (100 x 0.3) Micron Dual Gate FET.

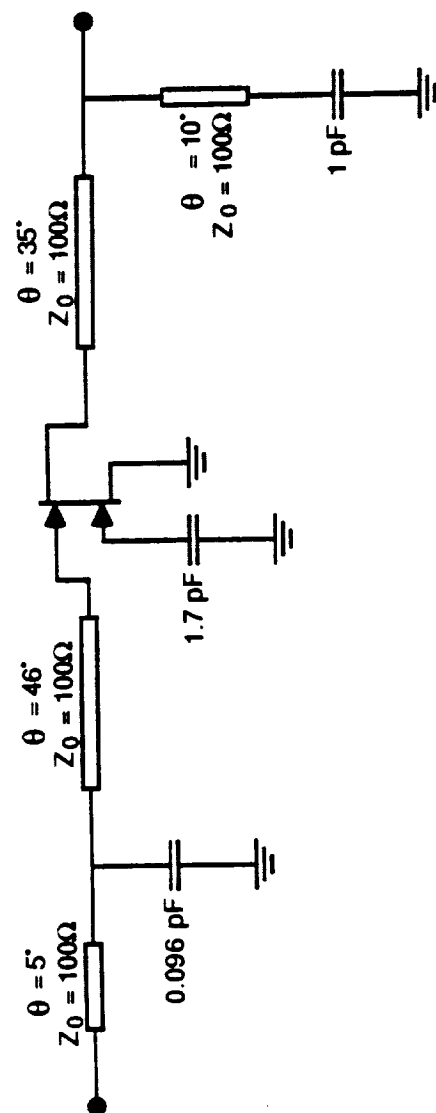


Figure 4. Circuit Diagram of Single Stage Gain Control Amplifier.

70400

ratios (>10) to be used in the output matching circuit owing to the high Q ($Q \sim 17$) of the dual-gate FET output network. To achieve a fractional bandwidth of at least 10% with a realizable microstrip circuit on a 6 mil GaAs substrate, an output VSWR of about 6 is required. Under these conditions a maximum gain of about 8 dB is predicted using the dual-gate FET equivalent circuit. Figure 5 shows the calculated result over the 27.5 to 30GHz band.

A circuit diagram of the two-stage gain control amplifier final design is shown in Figure 6. This design was developed using the latest dual gate FET equivalent circuit from DG43. The two-stage design was chosen for the following reasons:

- o Distributing the gain control over two stages rather than one reduces the total associated phase shift since phase shift in a dual gate FET varies less rapidly with gain changes at the upper end of the gain control range.
- o Noise figure degradation is minimized by avoiding large gain changes in either stage.

The gain control is adjustable at both stages by controlling the dc voltage applied to the second gates. For the 100 micron gate width devices used in the design, the magnitude of the output S-parameter, S_{22} , is nearly unity, and significant mismatch must be employed in the output and interstage networks to achieve reasonably flat gain. This fact, coupled with the impedance restrictions imposed by monolithic design (high impedance transmission lines are limited to $Z_0 < 100$ ohms), restrict the amplifier fractional bandwidth to about 10 percent. Larger gatewidths can reduce this problem at the expense of increased power consumption. The predicted performance of the two-stage amplifier is $8 \text{ dB} \pm 2 \text{ dB}$ gain over the 27.5-30 GHz band with gate 2 adjusted for maximum gain. The calculated response is shown in Figure 7.

1.3 Gain Control Amplifier DC and RF Results - Delivery

Two iterations of gain control amplifier designs based on there designed dual gate FET have been fabricated on ion implanted LEC GaAs wafers and evaluated. the initial evaluation of the first wafer run focused on the single stage gain

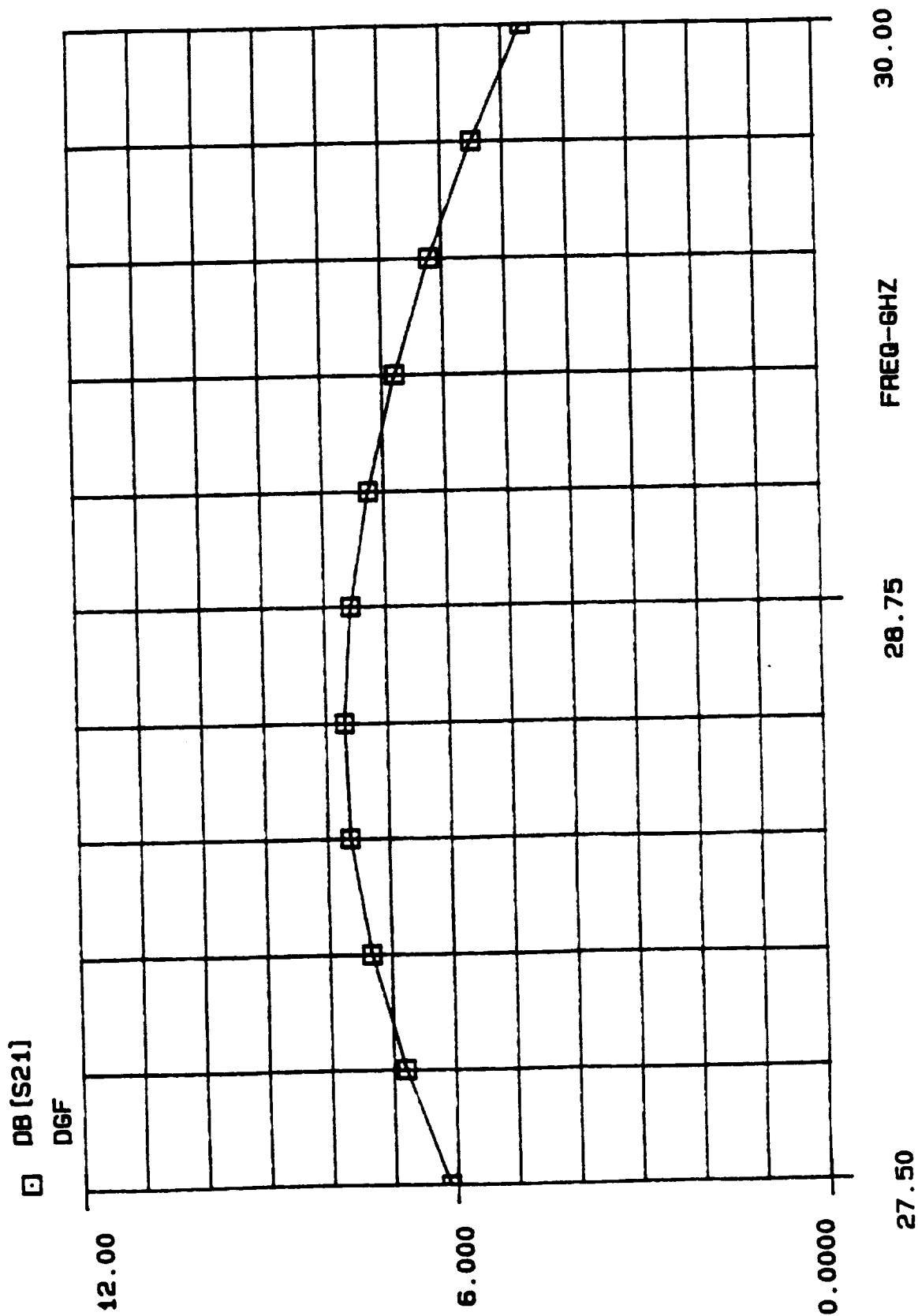
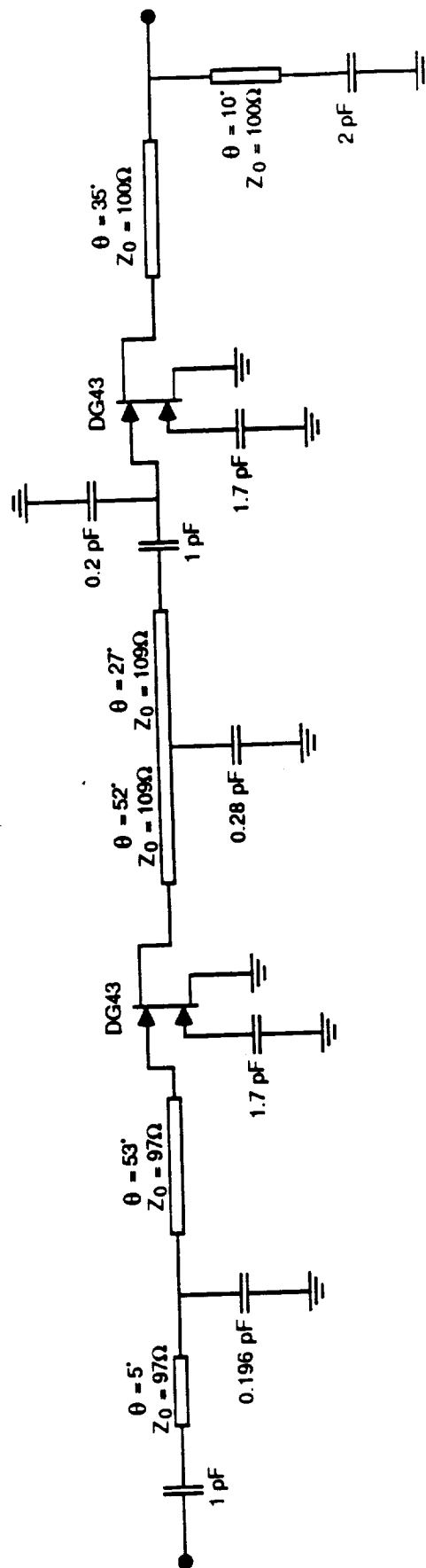


Figure 5. Calculated Response of One Stage Gain Control Amplifier.



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Figure 6. Circuit Diagram of Two-Stage Gain Control Amplifier Final Design.

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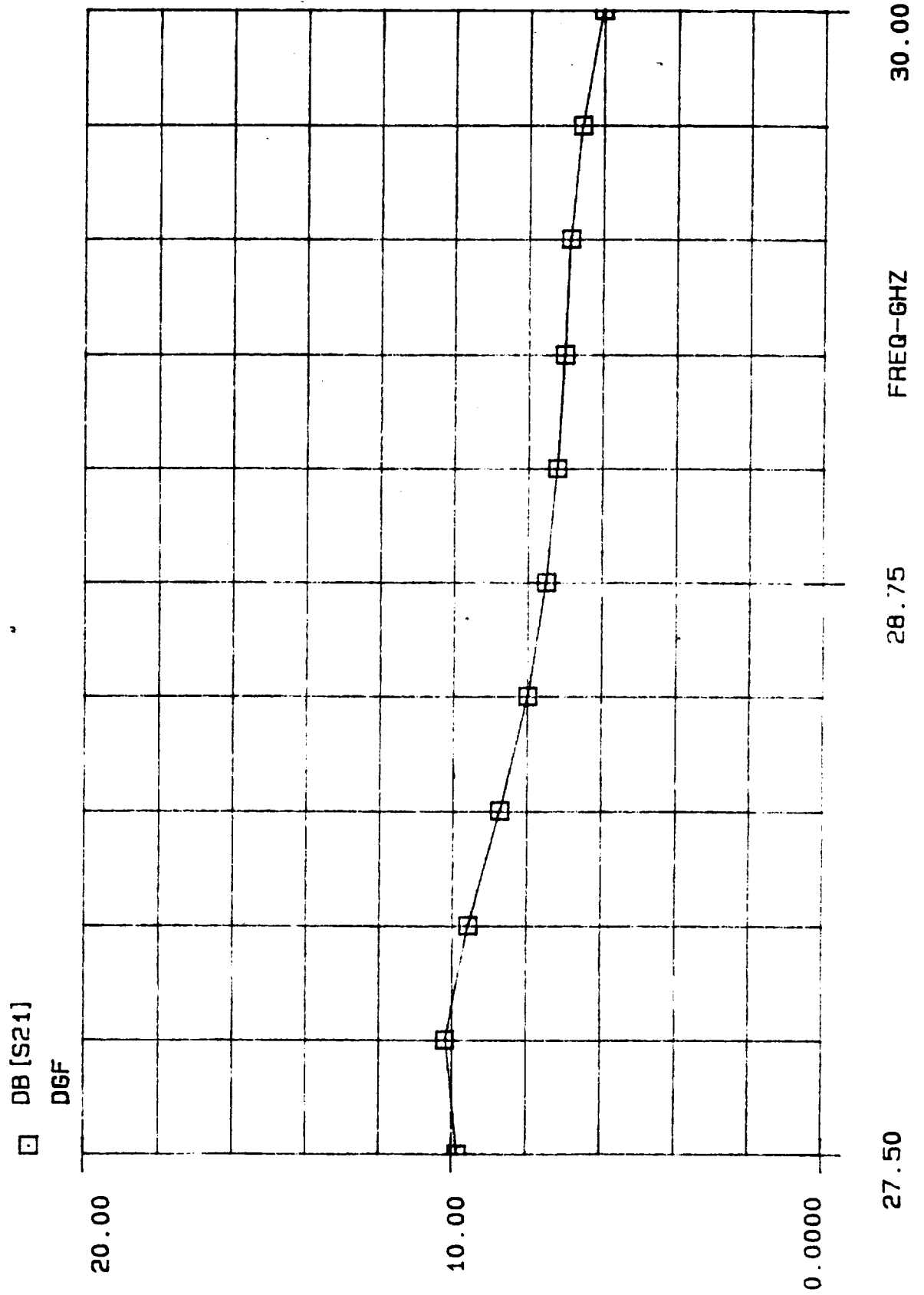
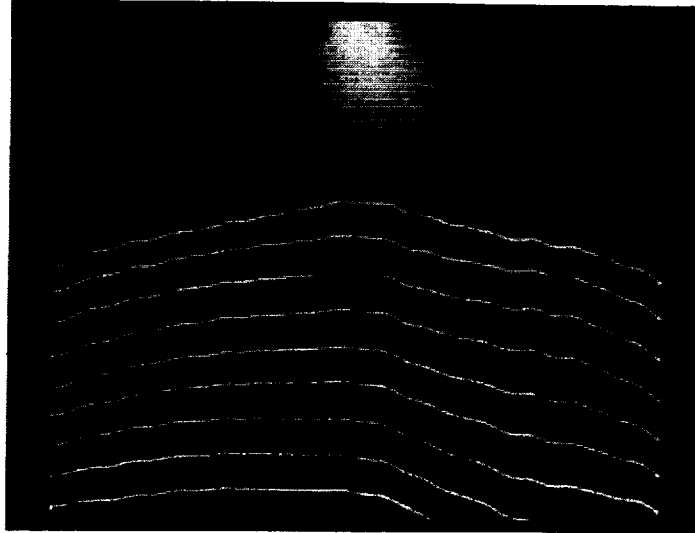


Figure 7. Calculated Response of Two-Stage Gain Control Amplifier Final Design.

control amplifier. A gain versus frequency plot for the single stage design is shown in Figure 8. By adjusting the voltage on the second gate from +0.96 V to -2.52 V, a gain variation of at least 24 dB can be obtained. As is obvious from Figure 8, the gain response is too high in frequency with respect to the 27.5 - 30 GHz NASA band. The main reason for the shift in operating band to higher frequencies is that the output capacitance of the actual device is smaller than the capacitance used in the equivalent circuit model. Nevertheless, the result demonstrated operation of a monolithic dual gate FET amplifier using quarter-micron gates in Ka-band. To our knowledge, this is the first such circuit demonstrated at these frequencies and this resulted in publication of a paper describing these results [1].

After obtaining the single stage results we proceeded to mount and evaluate the two-stage amplifier circuit. The initial response for the two-stage circuit is shown in Figure 9. The response of the two-stage amplifier is shifted to higher frequencies (centered around 32.6 GHz) as was the case with the single stage amplifier. However, the gain is less than for the single stage circuit. Following a series of experiments, modifications as shown in Figure 10 were made to the RF and biasing networks resulting in a significant improvement in performance of the two-stage design. To compensate for the lower device capacitance, the 100 ohm transmission lines in the interstage and output network were lengthened using bond wires. For the dc bias networks, an off chip resistor and capacitor were added to improve the bias isolation. With these changes, we achieved 12 dB gain centered around 29-30 GHz. During the modification, the first stage second-gate bypass capacitor was mechanically damaged (shorted) and further measurements had to be made with the second gate of the first stage at zero volts. RF data for the modified chip is shown in Figure 11 over the 27.5 - 30 GHz band. The frequency response is much improved and the maximum gain is 8 dB. The gain is limited by the inability to bias the second gate of the first stage FET. A partial delivery of the "best effort" gain control amplifier consisting of 47 amplifiers was made from this run. Based on the results of this second iteration, a third and final design was generated for the gain control amplifier using a revised equivalent circuit for the dual gate FET.

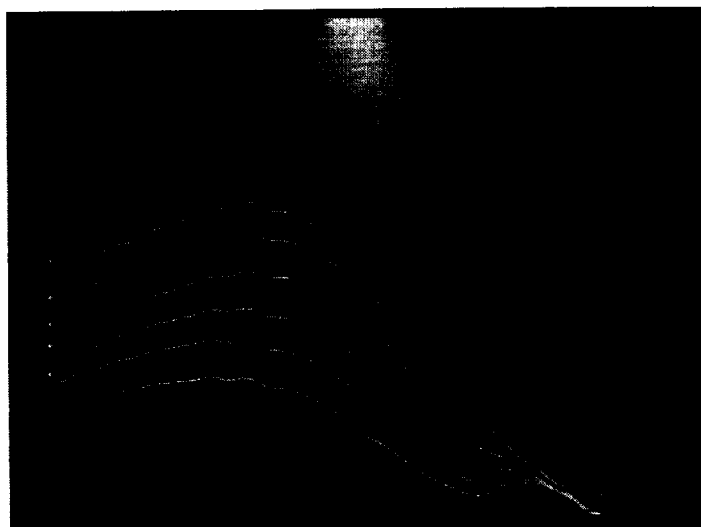


V_{G2} (V)	Gain (dB)
+0.96	+6
+0.34	+3
+0.06	0
-0.27	-3
-0.80	-6
-1.31	-9
-1.78	-12
-2.18	-15
-2.52	-18

Vertical: 5 dB/div
Reference: Center Graticule Line
Horizontal: 500 MHz/div; 28.5 - 33.5 GHz

$V_{DS} = 5.5$ V , $V_{G1} = 0.0$ V
 $V_{G2} = +0.96 \rightarrow -2.52$ V
 $I_{DS} = 22.5$ mA \rightarrow 1.8 mA

Figure 8. Gain versus Frequency for Single Stage
Gain Control Amplifier with Various Second
Gate Voltages



Gain (dB)	V_{G21} (V)	V_{G22} (V)
6	0.9	1.0
3	0.9	.38
0	0.9	.10
-3	.45	0
-6	.25	0
-9	0	0

Vertical: 5 dB/div
Reference: Center Graticule Line

Horizontal: 500 MHz/div; 30-35 GHz

For maximum gain:

<u>1st Stage</u>	<u>2nd Stage</u>
$V_D = 3.0V$	$V_D = 6.0V$
$I_D = 21.9 \text{ mA}$	$I_D = 23 \text{ mA}$
$V_{G11} = 0.0V$	$V_{G12} = 0.0V$
$V_{G12} = +0.9V$	$V_{G22} = 1.0V$

Figure 9. Gain Versus Frequency for Two-Stage Gain Control Amplifier with Various Second Gate Voltages

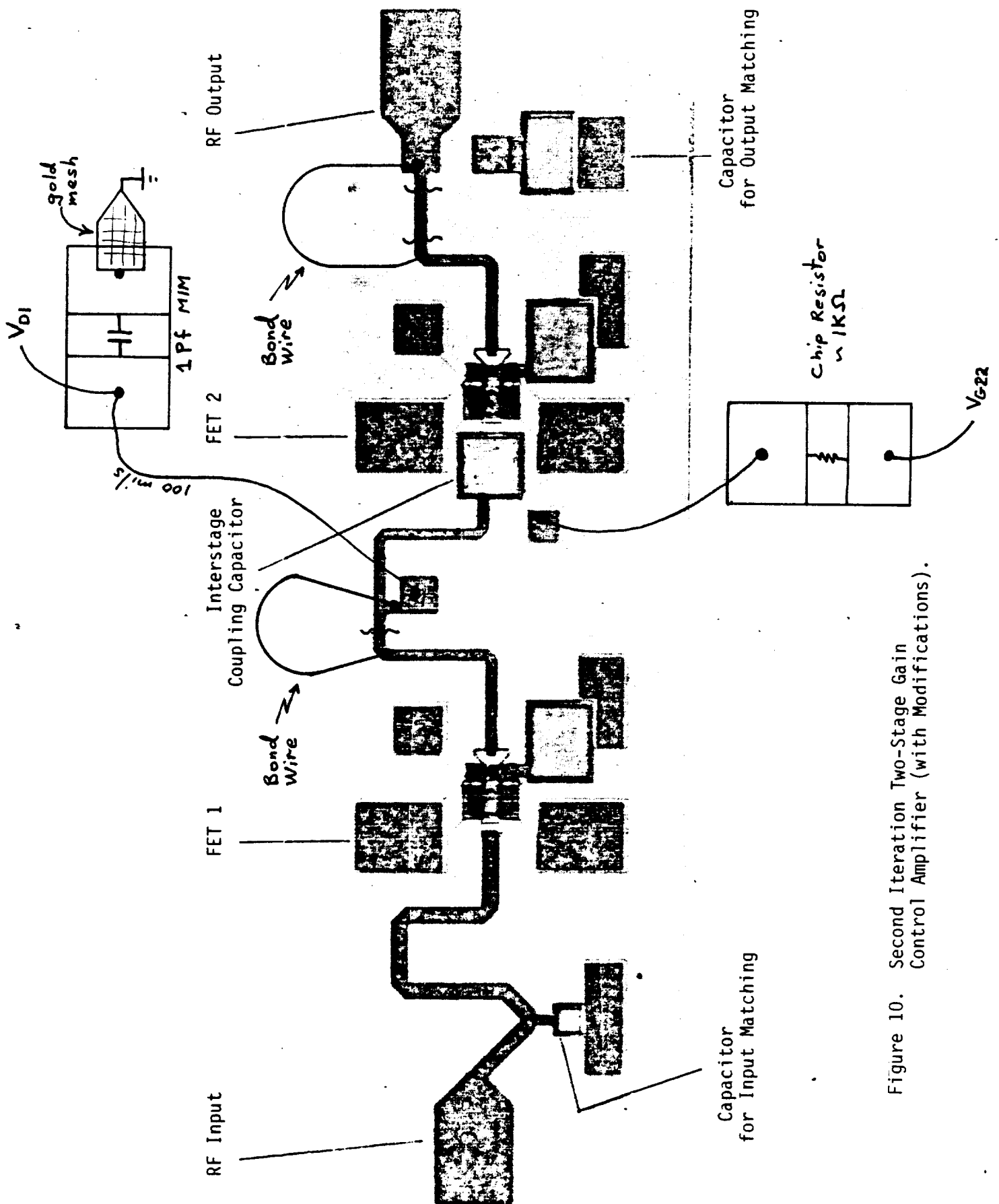
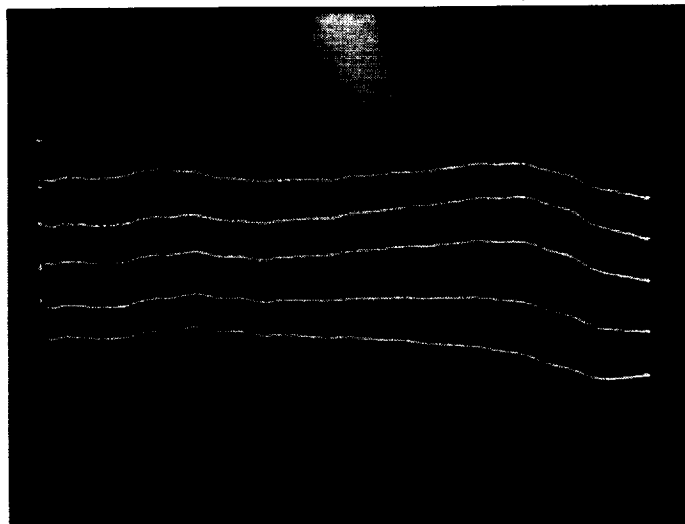


Figure 10. Second Iteration Two-Stage Gain Control Amplifier (with Modifications).



Gain (dB)	V _{G21} (V)	V _{G22} (V)
7	0	1.11
4	0	0.48
1	0	0.2
-3	0	-0.16
-6	0	-0.64

Vertical: 5dB/div
Reference: Center Graticule Line

Horizontal: 250 MHz/div; 27.5-30GHz

For maximum gain:

<u>1st Stage</u>	<u>2nd Stage</u>
V _D = 4.7V	V _D = 4.7V
I _D = 97 mA	I _D = 25.4 mA
V _{G11} = 0.93 V	V _{G12} = 0V
V _{G21} = 0V	V _{G22} = 1.11V

Figure 11. Gain versus Frequency for Two-Stage
Gain Control Amplifier (with modification)

The redesigned two-stage gain control amplifier layout is shown in Figure 12. This revised design contains options for modifying the input and output matching networks and an added input coupling capacitor. Four mask levels were remade to fabricate this design. The first four levels containing the alignment marks and FET design remained the same. A photomicrograph of the completed gain control amplifier chip is shown in Figure S-3.

Two-stage amplifiers of the final design were mounted for RF evaluation. Gain curves for an unmodified chip are shown in Figure 13. The peak amplifier gain of 12 dB occurs at 30 GHz with a 2 dB bandwidth of 400 MHz. The gain can be adjusted over a range of greater than 30 dB. This initial result was much closer to the design goals than the second iteration design. However, on chip modifications were still required to center the amplifier in the 27.5 - 30 GHz NASA band. The modifications made on the final design are shown in Figure 14.

RF performance for the modified amplifier is shown in Figures 15 and 16. The modified amplifier has a gain of 12 dB at center band. The 2 dB bandwidth of the amplifier is 2 GHz which is somewhat less than the designed 27.5 - 30 GHz. The attenuation levels of -3 dB, -6 dB, -10 dB, and -13 dB are achieved as shown in Figure 15. The phase shift envelope for the circuit is shown in Figure 16. The phase shift envelope at center band is less than 20 degrees as the gain changes over the desired range. At the 27.5 GHz band edge, the envelope increases to approximately 45 degrees. Input return loss is greater than 5 dB over most of the band; output return loss is poorer due to the high output impedance of the dual gate FET. These results on the 2-stage amplifier have been reported in a 1987 symposium paper [2].

The delivery of the remaining 53 gain control amplifier (55 were actually delivered) were made from the third iteration design. The data shown was for an amplifier from wafer DG 85. The performance of the amplifiers in terms of operating frequency range is highly correlated with the input capacitance (C_{gs}) of the amplifier FETs. Table 1 compares the input capacitance and gate length for a number of wafers. All except DG43 are wafers from the latest amplifier run. An amplifier from wafer DG85 was selected for evaluation since its input capacitance (measured at $V_{ds} = 0$ using 0 capacitance meter) most closely matched wafer DG43 which was used to gather data used for the

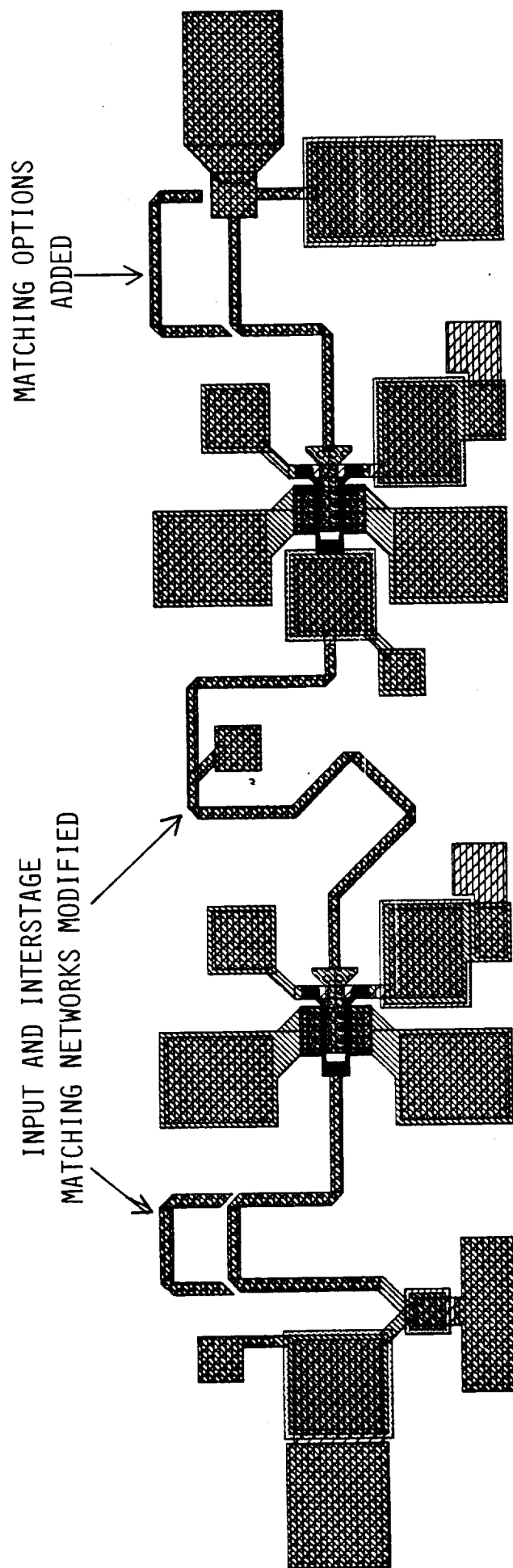
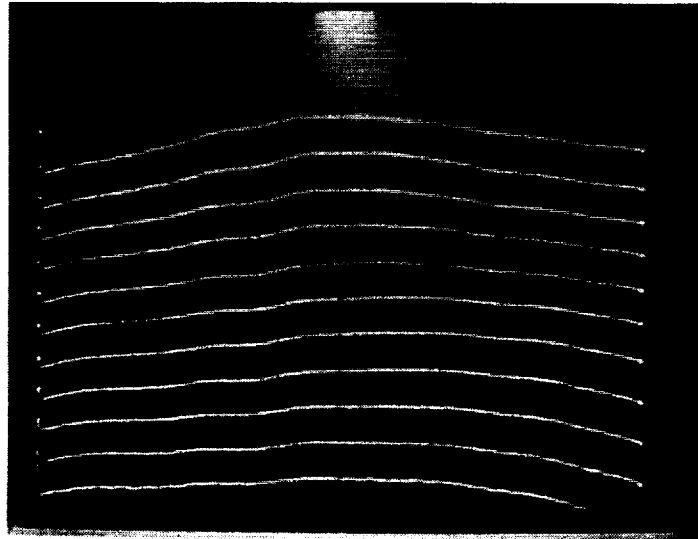


Figure 12. Third Iteration Gain Control Amplifier Layout.



Frequency: 29 - 31 GHz
Vertical: 5 dB/div
0 dB ref - center line

Figure 13. Gain vs. Frequency Characteristics for Final Design Two-Stage Gain Control Amplifier (Superposition of Several Gain States).

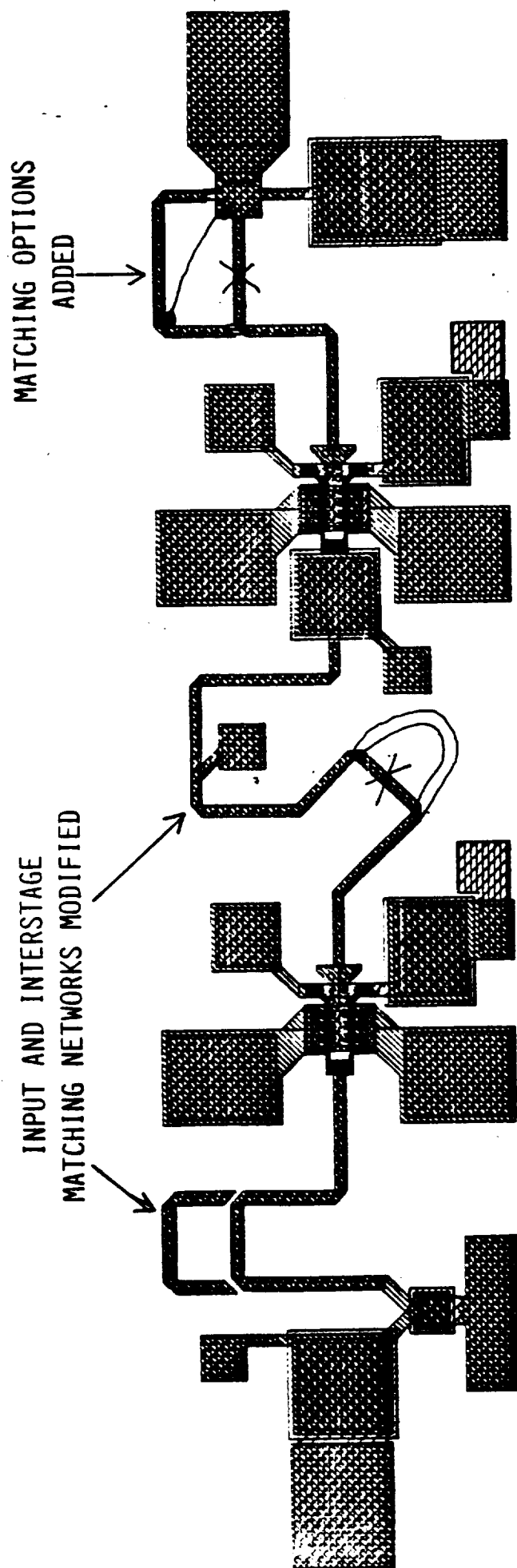
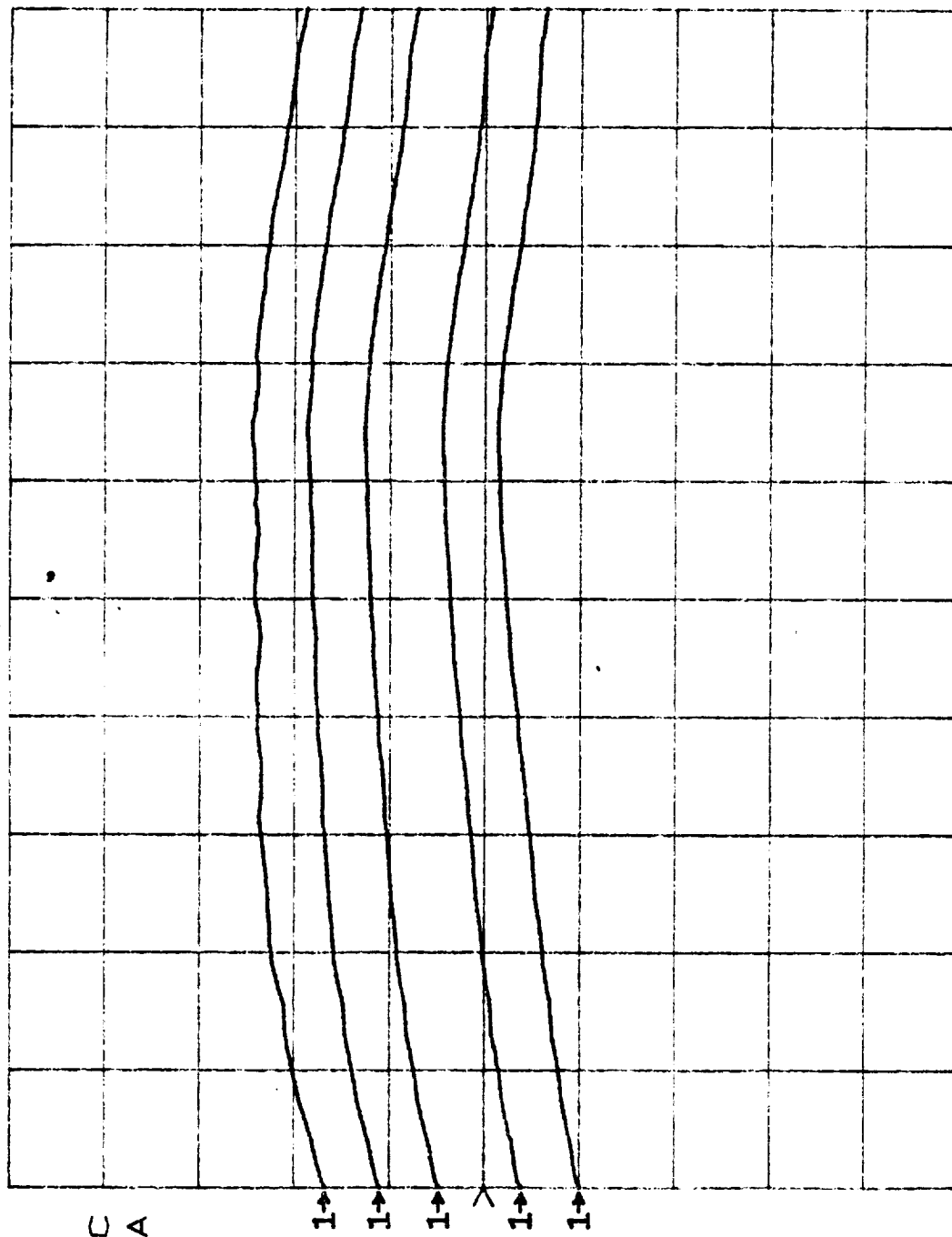


FIGURE 14. TWO STAGE GAIN CONTROL AMPLIFIER FINAL DESIGN WITH ON-CHIP MODIFICATIONS

S21 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

FIGURE 15. GAIN VS. FREQUENCY FOR GAIN CONTROL AMPLIFIER FINAL DESIGN
 WITH ON-CHIP MODIFICATIONS.

**TABLE I. VARIATION OF INPUT CAPACITANCE AND GATE LENGTH
FOR GAIN CONTROL AMPLIFIER WAFERS**

WAFER NUMBER	INPUT C	GATE LENGTH
DG43 (OLD DESIGN)	.110 pF	.35 MICRON
DG71	.116 pF	.36 MICRON
DG72	.096 pF	.26 MICRON
DG74	.091 pF	.29 MICRON
DG83	.128 pF	.28 MICRON
DG85	.120 pF	.28 MICRON

redesign. Amplifiers from other wafers may require more modification than amplifiers from DG85. In the future, improved process control and circuit designs with more tolerance to device variations must be developed to avoid the need for on-chip modifications.

1.4 Two-Stage Low Noise Amplifier Design

The two-stage low noise amplifier design is based on a 0.25 x 100 micron gate ion implanted MESFET. The FET model used in the two-stage amplifier design is shown in Figure 17. The element values in the model are based on experimental S-parameter measurements made on early FETS over the 2-12 GHz frequency range. The monolithic circuit designs were done using COMPACT and later verified using Touchstone. The amplifier circuit and calculated response are shown in the third annual report, page 26.

1.5 Low Noise Amplifier DC and RF Results - Delivery

Low noise amplifiers and discrete FETs were fabricated on the same wafers as the gain control amplifiers. The low noise amplifier design is based on a 0.25 x 100 micron single gate FET. A photomicrograph of the 2-stage LNA is shown in Figure S-4. The chip size is 2.3 x .71 x .015 mm³. A dc drain I-V for a typical amplifier FET is shown in Figure 18. Devices have a maximum dc transconductance of 120-150 mS/mm. S-parameter measurements were taken on discrete devices to develop an equivalent circuit model for the FETs. Figure 19 shows a FET equivalent circuit for devices from wafer DG 43. This model will be used to develop future generation designs of the low noise amplifier for the CTS receiver.

To characterize the ion implanted FETs in terms of noise figure, a hybrid amplifier utilizing a discrete 0.25 x 100 micron gate device was assembled and tested. Figure 20 shows the results of these tests. The best noise figure is 4.5 dB with an associated gain of 4 dB at 34 GHz. Although this noise figure meets the program requirements, the gain is short of the 6 dB goal by about 2 dB.

To further establish the noise properties of the FETs we obtained a set of Ku-band noise data to determine the four noise parameters: F_{min} , R_{op} , X_{op} , and

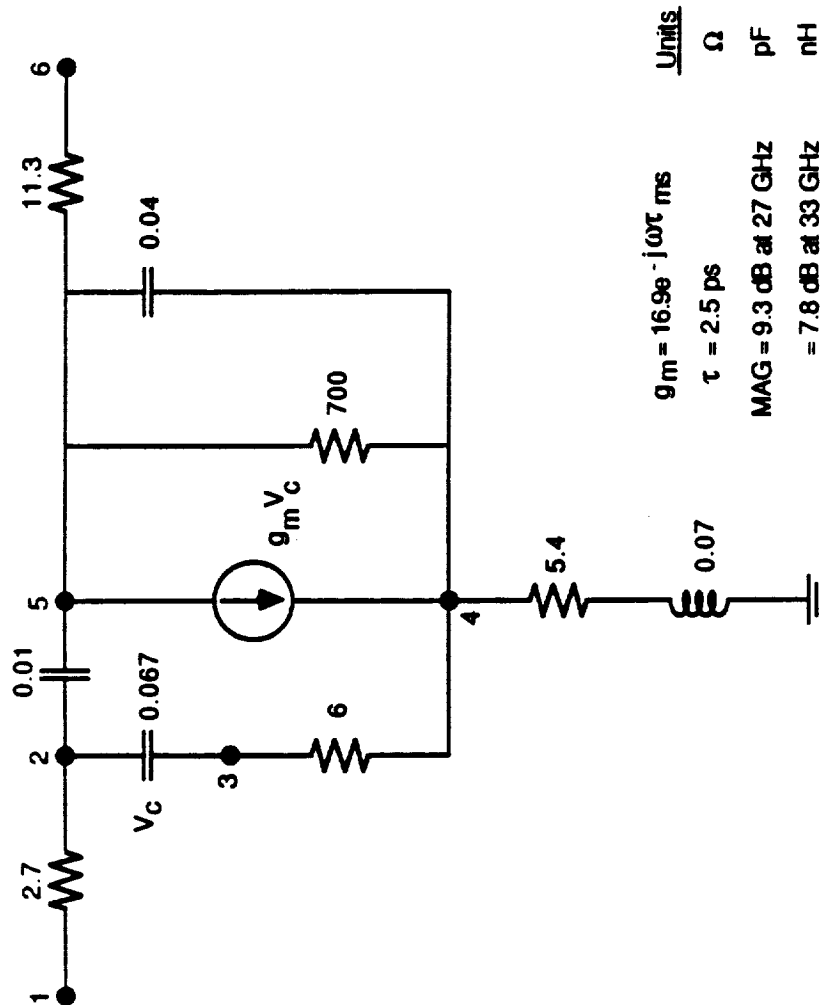
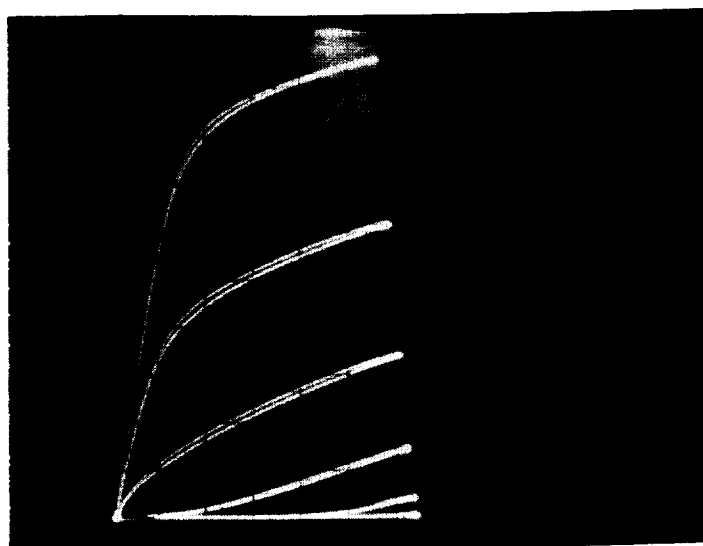


Figure 17. Low Noise FET Equivalent Circuit.



2ma/div - vertical
.5V/div - horizontal
.5V/step

Figure 18. DC Drain IV of .25 x 100 Micron Gate FET
on Same Wafer.

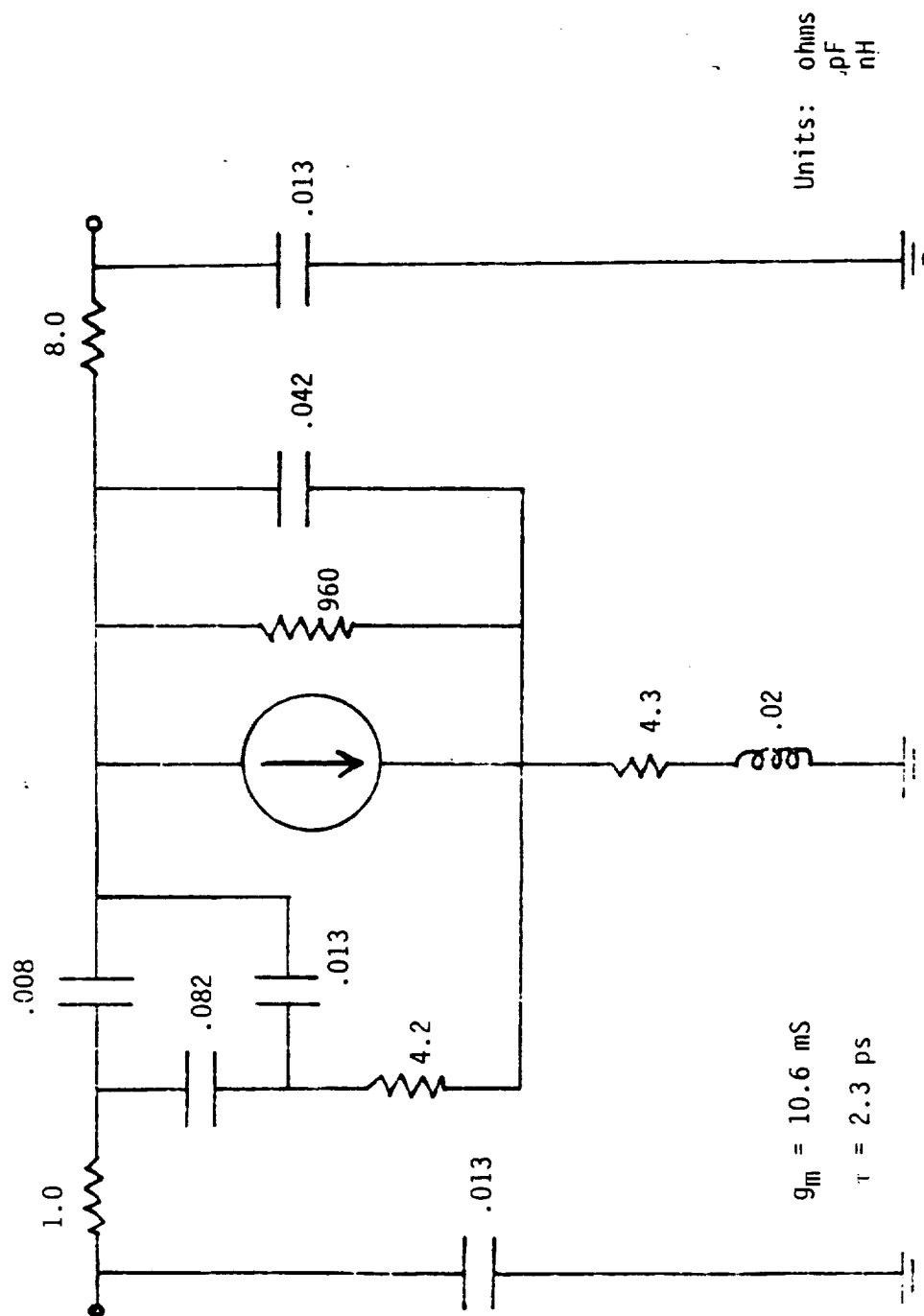


Figure 19. Equivalent Circuit for Ion-Implanted 0.25 x 100 Micron FET (DG43) at 44% I_{DSS} (Revised).

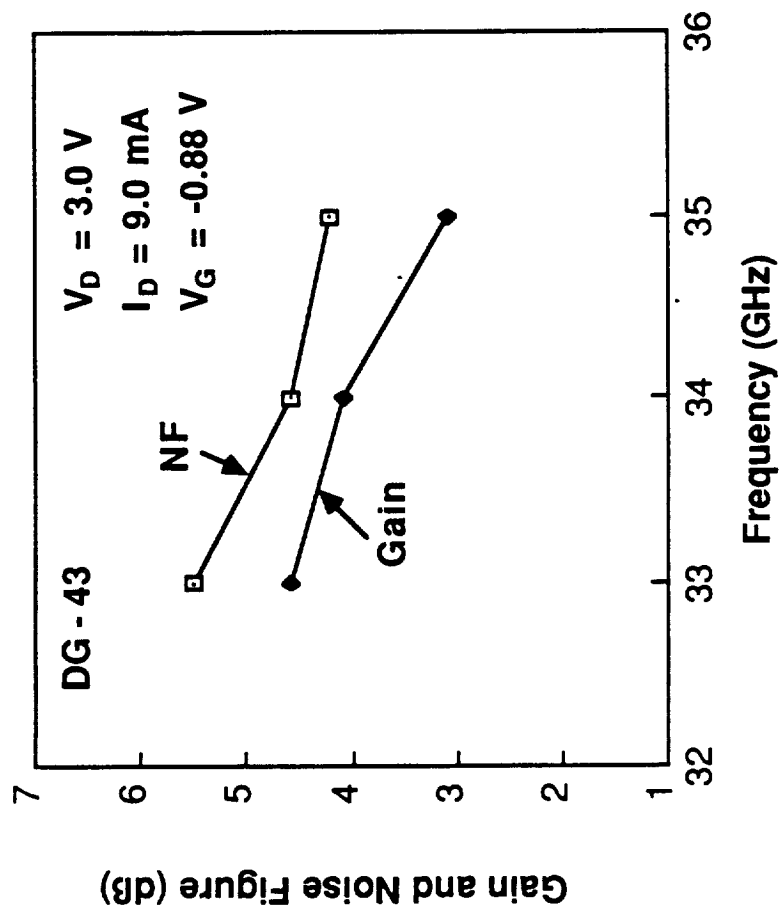


Figure 20. Noise Figure Data and Associated Gain for Ion Implanted 0.25 x 100 Micron FETs (DG43) in Ka-Band.

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R_n . Noise measurements were made at three different generator impedances $R_g + jX_g$. The noise parameters were then determined from the general noise figure formula:

$$F = F_{min} + R_n \frac{[(R_g - R_{op})^2 + (X_g - X_{op})^2]}{R_g (R_{op}^2 + X_{op}^2)}$$

A noise resistance, R_n , of 490 ohms was determined from these measurements. The data was also used to generate a plot of constant noise circles as shown in Figure 21. Note that the minimum noise figure achieved was 1.9 dB with 7.2 dB associated gain. We intend to extend these measurements to Ka-band in the future to develop data on the optimum source impedance for our low noise devices. We believe that the key to obtaining improved performance from our low noise amplifier is in improving the input circuit noise matching and the performance of the device itself.

As was the case with the dual gate amplifier, the 2-stage low noise amplifiers required on-chip modification for operations in NASA band. Figure 22 shows the gain and input return loss for an LNA from wafer DG85 before and after modification. Before modification, the amplifier had a double peaked response. The higher frequency peak corresponded to a peak in the input and output return loss. From this data it was surmised that the lower frequency peak was related to the interstage matching and the high frequency peak was related to the input and output matching. This information formed the basis for on-chip modifications. The input and output matching circuits on the chip were modified with wire bonds as shown in Figure 23. The resulting amplifier response is shown in Figure 22b. With these modifications the LNA achieved 7dB gain with a 6.2 dB noise figure at the chip level. A total of ten unmodified 2 stage LNA chips were delivered to NASA. A modified version of the LNA was used in the receive module delivered to NASA. The low gain of the LNA caused a high overall noise figure for the receive module. In the future, LNAs with a larger number of stages will be developed to reduce the overall receiver noise figure as described in section 3.3 on the CTS receiver development.

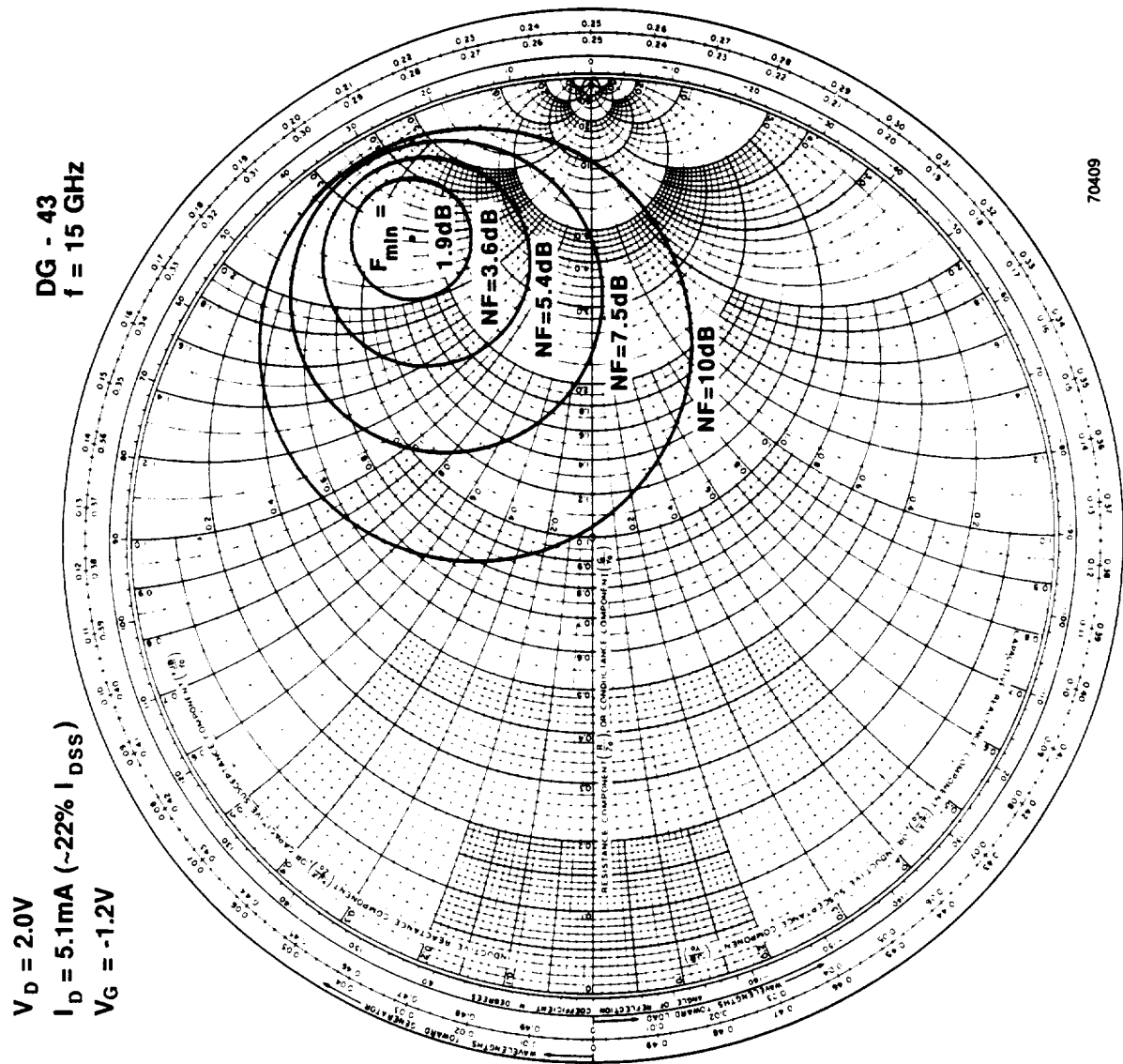
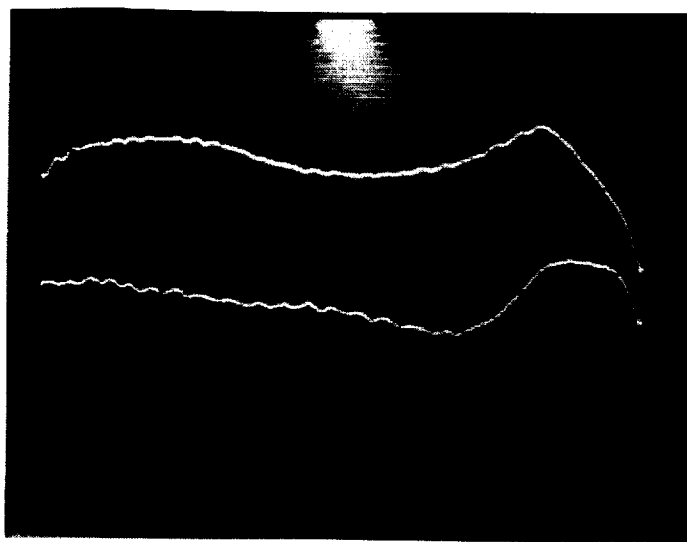
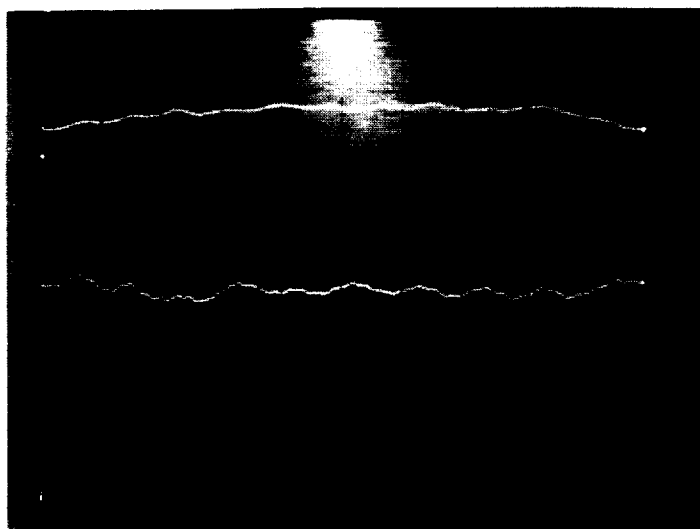


Figure 21. Constant Noise Figure Circles Measured for an Ion-Implanted 0.25 x 100 Micron Gate FET.



A) UNMODIFIED LNA

GAIN - TOP TRACE
 INPUT RETURN LOSS - BOTTOM TRACE
 HORIZONTAL 27-37 GHZ
 VERTICAL GAIN 5DB/DIV
 RETURN LOSS 10DB/DIV
 CENTERLINE 0DB
 BIAS $V_{G1} = -0.4V$
 $V_{G2} = -1.61V$
 $V_{D1} = 2.7V$
 $V_{D2} = 3.0V$
 $I_{D1} = 37.5 \text{ MA}$
 $I_{D2} = 23.2 \text{ MA}$



B) LNA AFTER MODIFICATION

GAIN - TOP TRACE
 RETURN LOSS - BOTTOM TRACE
 HORIZONTAL 27.5-30 GHZ
 VERTICAL GAIN -5DB/DIV
 RETURN LOSS 10DB/DIV
 BIAS $V_{G1} = -.64V$
 $V_{G2} = -1.94V$
 $V_{D1} = 3.49V$
 $V_{D2} = 2.70V$
 $I_{D1} = 34 \text{ MA}$
 $I_{D2} = 23.3 \text{ MA}$

FIGURE 22. RESPONSE OF LNA FROM WAFER DG 85 BEFORE AND AFTER MODIFICATION.

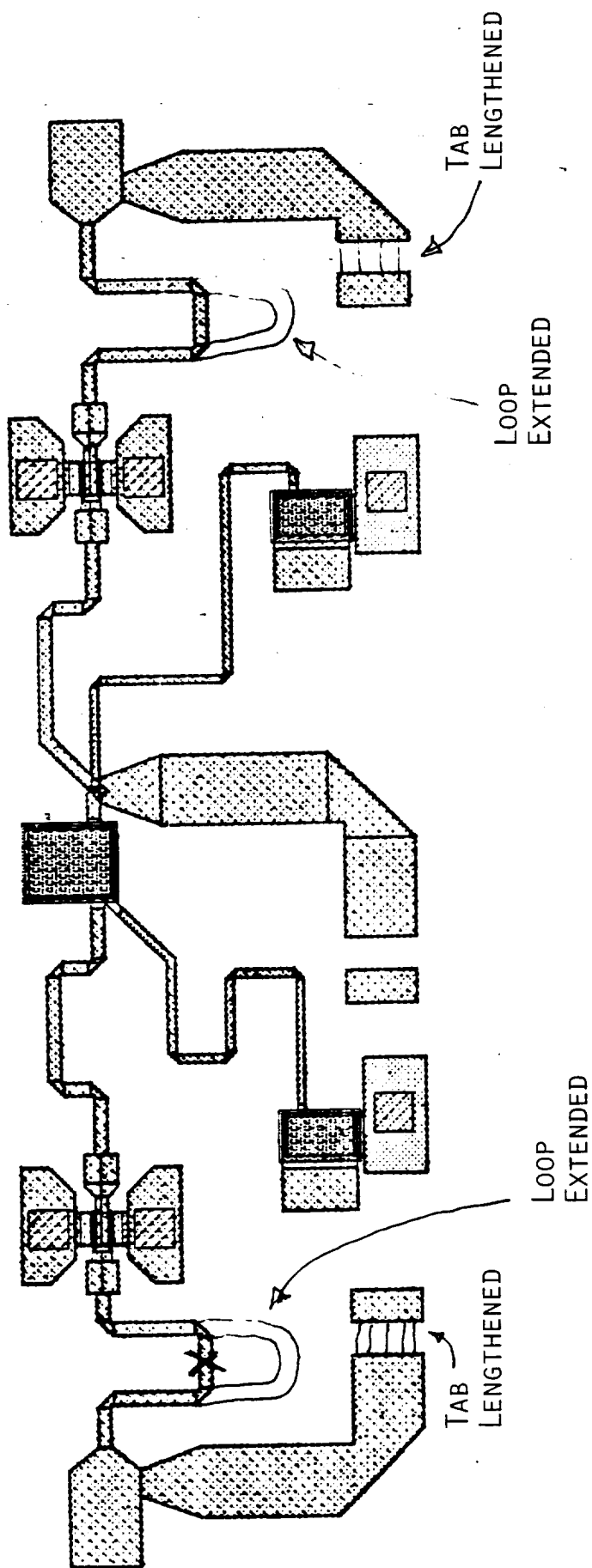


FIGURE 23. ILLUSTRATION OF MODIFICATIONS TO LNA CHIP

2.0 RF/IF Development -- Task IV

This section contains a description the design and fabrication of all of the circuit elements used to convert the 27.5 - 30 GHz signal frequency to the 5.5 - 8 GHz IF frequency. The subsections contain:

- o Description of the e-beam/optical projection lithography process used to fabricate all of the RF/IF circuit elements
- o Microdot mixer diode
- o 30 GHz monolithic balanced mixer
- o IF amplifier
- o 22 GHz LO amplifier
- o Status and plans

2.1 E-beam/Optical Projection Lithography Fabrication Process

Two quite distinct device structures are used in the RF/IF module. The local oscillator reference and IF amplifiers need submicron FETs and the mixer requires high cutoff-frequency Schottky mixer diodes. The first device has a very shallow active layer with an abrupt doping profile between the active layer and the substrate. The second employs a thick contact layer with a relatively abrupt doping profile near the surface. With proper designs both of these devices can be fabricated using ion implantation. To realize these designs, however, a fabrication process with excellent alignment capabilities is needed. A process developed under Honeywell IR & D funds with these capabilities is described in this subsection.

The 0.5 and 0.25 micron gate lengths needed for low noise operation at 8 and 22 GHz, respectively, are defined using e-beam lithography in our process. All other levels are defined by optical lithography to reduce the ultimate cost of fabrication. While there are many factors which contribute to process yield, the ± 0.2 micron alignment capabilities of the Censor direct-step-on-wafer projection lithography system are essential for fabricating the mixer diodes. The series resistance of these diodes is reduced by using the

parallel combination of 21 one-micron Schottky contacts. The alignment between the airbridges and the Schottky contacts must be very good for high yields. This system provides the proper alignments.

A flow chart of the process is given in Figure 24 with selected process steps described in greater detail in Figure 25. After defining the optical alignment marks on the wafer, the FET channel and mixer diode active regions are implanted. Following capping with silicon nitride the wafer is annealed and the cap removed. Ohmic contacts and the e-beam fiducials are defined and alloyed just prior to e-beam lithography. The e-beam lithography system writes the gate patterns after compensating for any variation between the patterns on the wafer and its own coordinate system. After depositing and lifting the gate metal, the first level circuit metal and mixer diode Schottky contacts are fabricated. Depositing capacitor and passivation dielectric and etching the dielectric where required is the last step before fabricating airbridges and the final circuit metal. When the circuit and airbridges have been plated the wafer is thinned and the substrate via mask aligned to frontside pads using an infrared aligner. The vias are etched with a chemically assisted ion beam etcher. After removal of the via resist with an oxygen plasma, a sputtered plating base layer is deposited over the backside of the whole wafer. Selective plating is used to define the streets for subsequent scribing and die separation.

2.2 Microdot Mixer Diode

A key element in the RF/IF is the microdot mixer diode. Fabrication of this diode is quite compatible with that of ion implanted FETs yet its performance is comparable to that of conventional diodes fabricated using epitaxial structures. The structure of the diode is indicated in Figure 26. In the current design it consists of 21 one-micron diameter Schottky contacts connected by an airbridge for minimum parasitic capacitance. A single Schottky contact typically has a junction capacitance of 2.6 fF and a series resistance of 84 ohms. This corresponds to a cutoff frequency greater than 700 GHz which is more than required for this application. Paralleling 21 of these contacts results in a diode with about .055 pF junction capacitance, 4 ohms series resistance and a parasitics "package" capacitance of .013 pF.

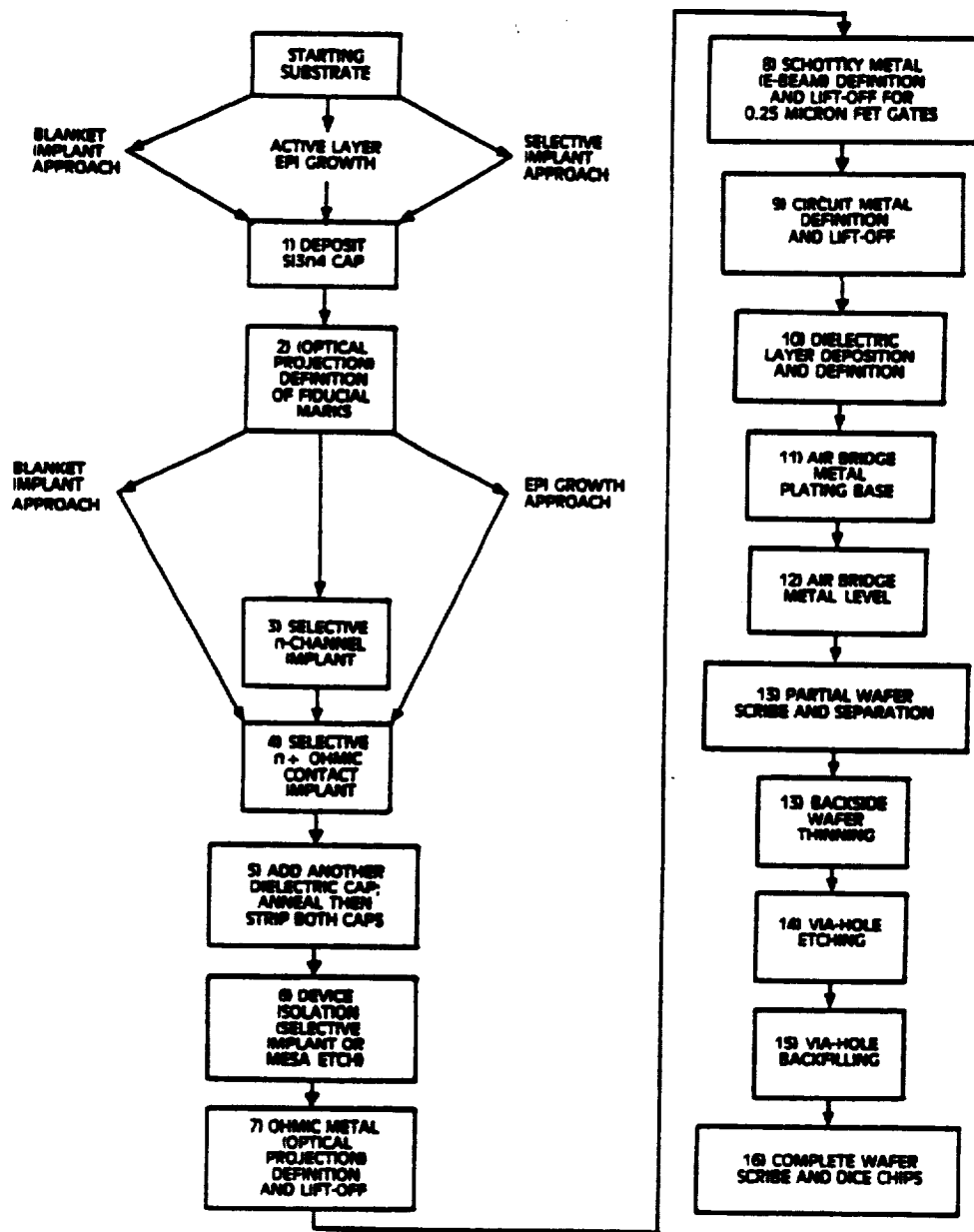


Figure 24. Flowchart for Honeywell's Electron-Beam/Optical Projection MIMIC Process.

Mixer Diode Low-Noise FET

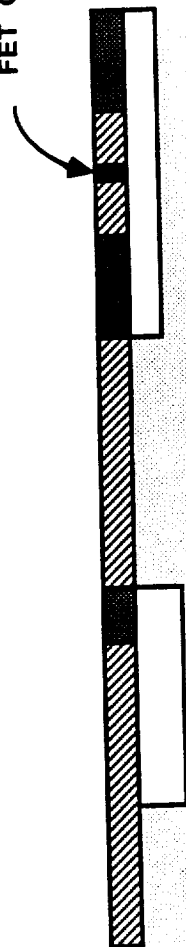


Implant and Anneal,
Remove Cap

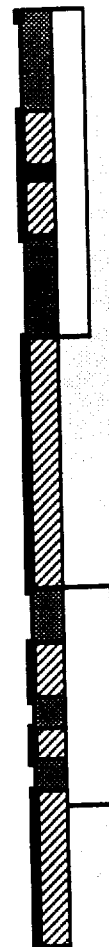


Ohmic Contacts

FET Gate

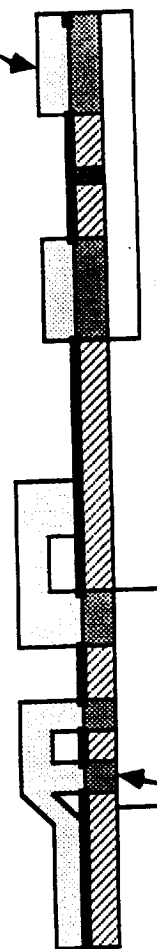


Si_3N_4 Deposition After
FET Gates



1st Circuit Metal

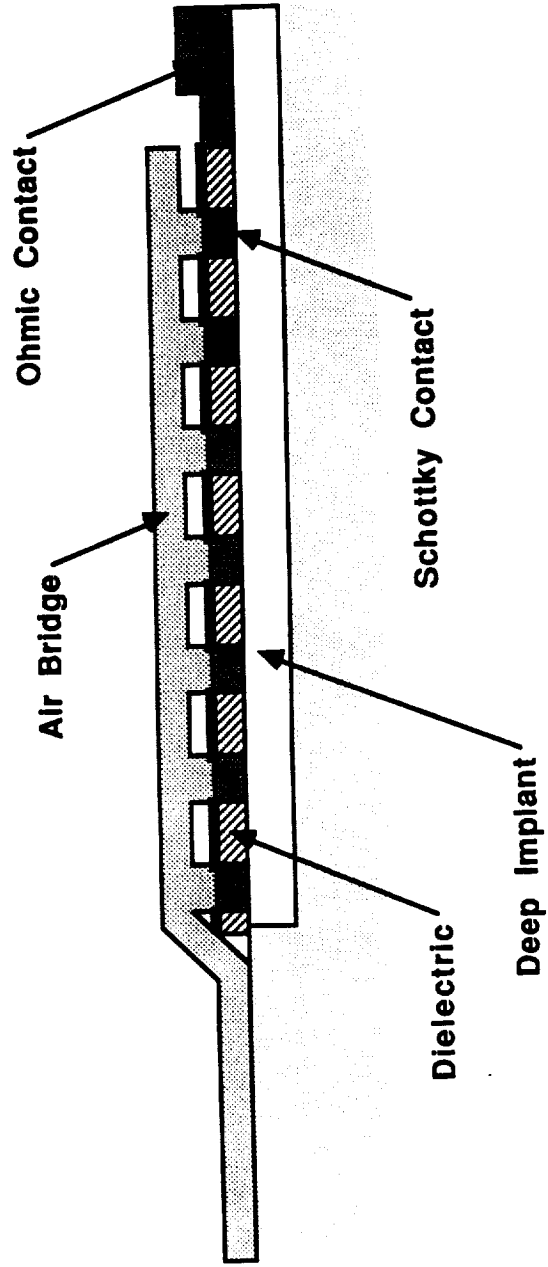
Circuit
Metal



Air Bridge Plating

Schottky Contacts

Figure 25. Selected Process steps in RF/IF Fabrication Process.



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Figure 26. Cross Section of Ion Implanted Diode Structure.

Measured I-V characteristics of one of the diodes is shown in Figure 27. The total zero-volt bias capacitance of the test structure, including pads, connecting lines and the diode itself was .0652 pF. The capacitance of a similar, nearby structure without Schottky contacts was .0135 pF. Assuming that the junction capacitance is equal to the difference, it is .0517 pF. The total series resistance of the structure including contact, probe, wiring and that of metal lines to the diodes is about 7 ohms. The measured resistance between two probes on a metal pad was 2 ohms. Neglecting the resistance of the metal lines this gives a diode series resistance of 5 ohms. The ideality of this particular diode was 1.06. A photo of the I-V characteristics of a similar diode is shown in Figure 28. The parameters measured indicate that the diode is not a very significant factor in the mixer conversion loss.

2.3 30 GHz Monolithic Balanced Mixer

There are some constraints on the monolithic mixer design:

- o Being ultimately fabricated on the same substrate as low noise FET amplifiers makes microstrip circuits strongly desirable for compatibility.
- o Fabrication must be compatible with submicron FET processes.
- o High IF frequency implies a wide bandwidth mixer to accommodate the signal, local oscillator and IF frequencies.

The latter is the most difficult since it requires controlled circuit impedances from the lowest IF frequency up to at least the sum of the local oscillator and signal frequencies. The design which provides all of these characteristics is shown in Figure 29. It consists of a broadbanded rat race hybrid, two diodes, matching circuits and IF output filter. Circuit grounds were the most troublesome element of the design. There are essentially two choices:

- o IF ground on side of the diodes away from the hybrid ring, or,
- o Connecting the hybrid ring to ground for IF frequencies

The first alternative requires that the hybrid ring be part of the IF circuit or that a multiple stage high pass filter be installed between the diodes and the hybrid ring. Neither is attractive. The dimensions of the hybrid ring are significant at the IF frequency making flat response hard to achieve if it is not grounded. With many elements, a high pass filter is lossy. With few components it is ineffective.

The second alternative with a stub which is relatively short at IF frequencies to ground the ring is preferable. This eliminates most of the IF frequency problems. It does require LO and signal frequency grounding with filters on the side of the diode away from the hybrid ring. They have a minor effect on the frequency response. The quarter-wave IF grounding stub impedance is a compromise between the most effective IF frequency ground and minimum loading of the hybrid ring at the local oscillator and signal frequencies. These factors may reduce the maximum achievable IF frequency as indicated by the calculated insertion loss for a small local oscillator power as described in Figure 30. This figure indicates that the diodes receive a balanced drive over the required bandwidth but tuning is quite critical. With increased local oscillator drive, this is not such a problem and the bandwidth of the mixer is quite adequate.

Performance was evaluated using a 22 GHz oscillator borrowed from the (then) Honeywell Santa Barbara Microwave Center for the local oscillator source. The conversion loss versus signal and IF frequency for one of these mixers is shown in Figure 31. The local oscillator power incident on the mixer was 13 dBm at 22 GHz but not all of this power is absorbed by the Schottky diodes. Figure 32 indicates that the minimum conversion is achieved for this power level. For a 30 MHz IF frequency with a 28.75 local oscillator similar results are obtained as indicated in Figure 33. All of the results include fixture and transition losses.

The mixers developed for this program have demonstrated:

- o IF frequencies higher than any other completely planar microstrip mixer
- o Ion implanted mixer diode cutoff frequencies beyond those of any other diodes

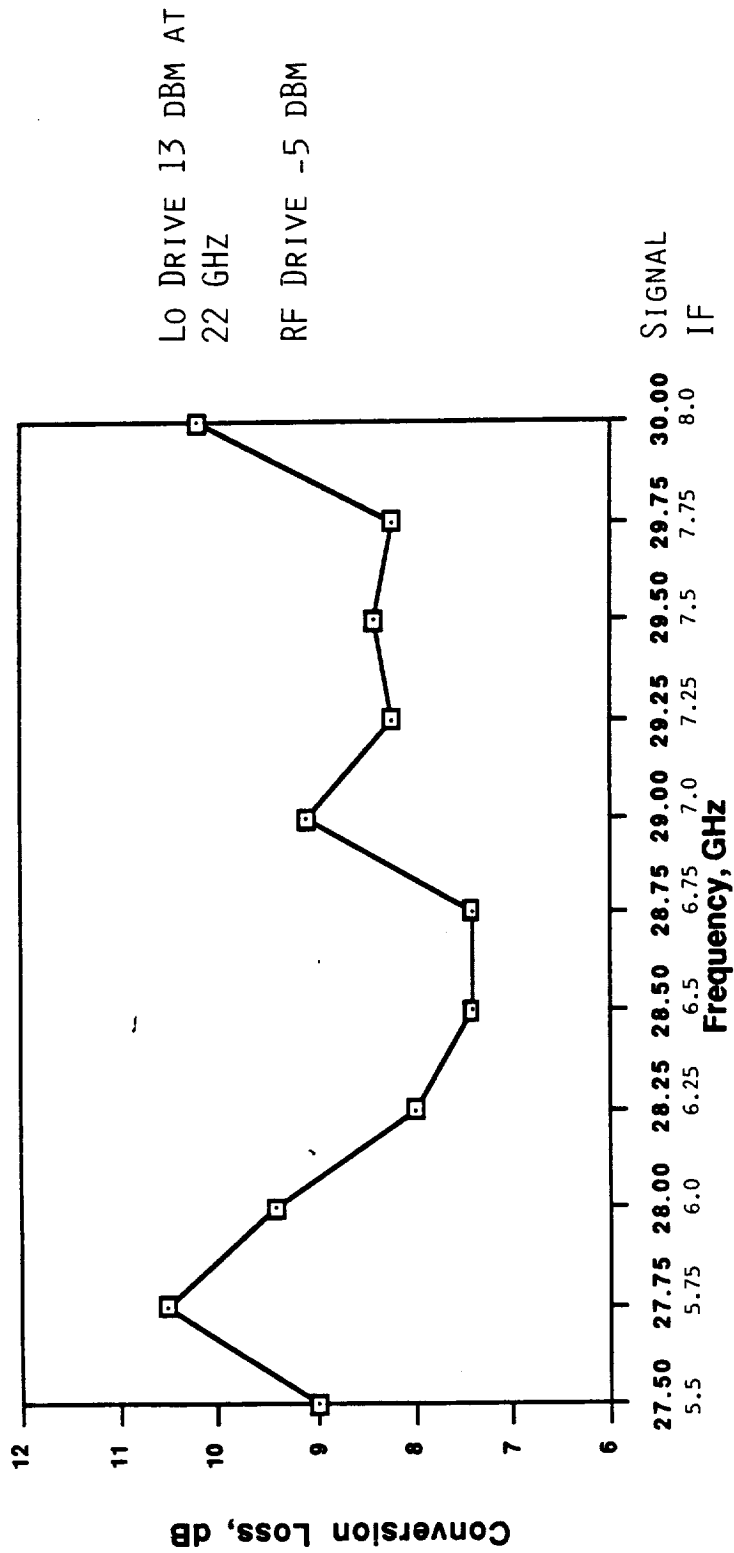


FIGURE 31. CONVERSION LOSS VS. FREQUENCY FOR ION IMPLANTED MODIFIED RAT RACE MIXER SHOWING HIGH IF FREQUENCY

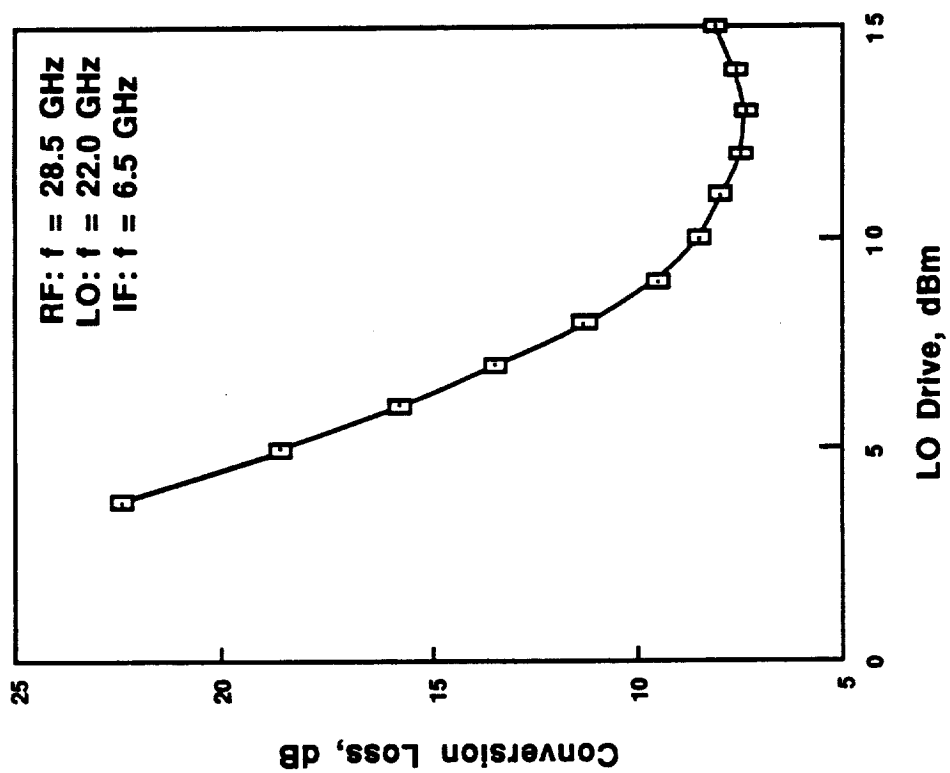


FIGURE 32 CONVERSION LOSS VS. LO DRIVE INDICATING
 BEST MIXER OPERATION FOR 13 DBM LOCAL OSCILLATOR
 DRIVE

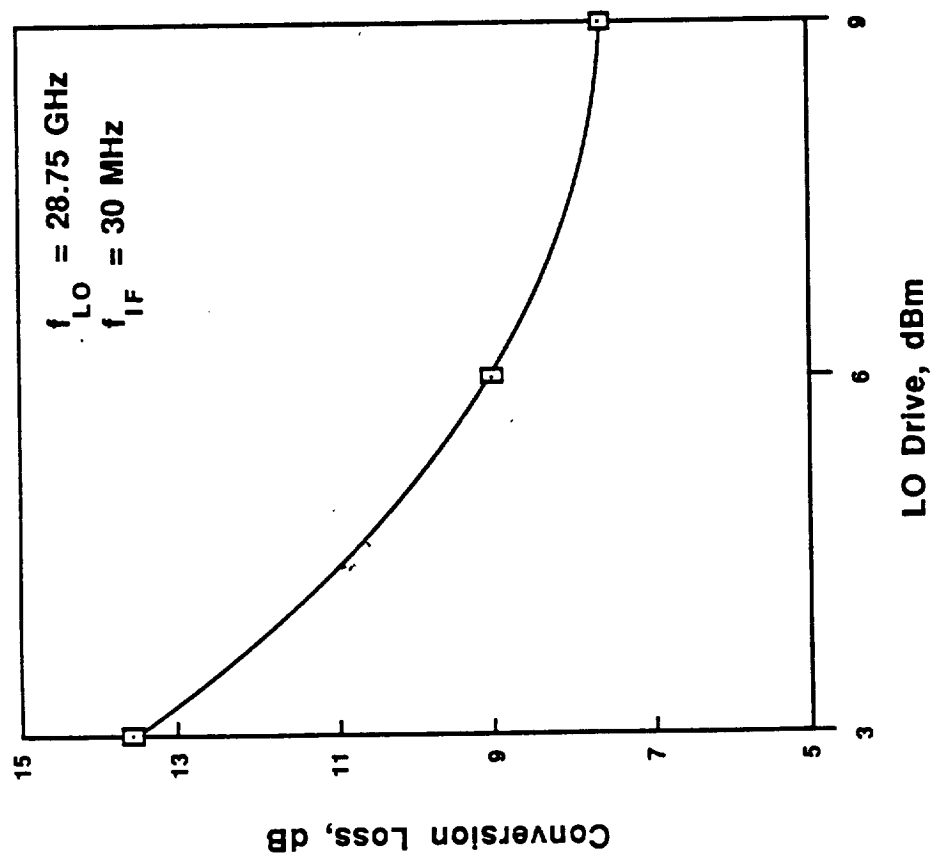
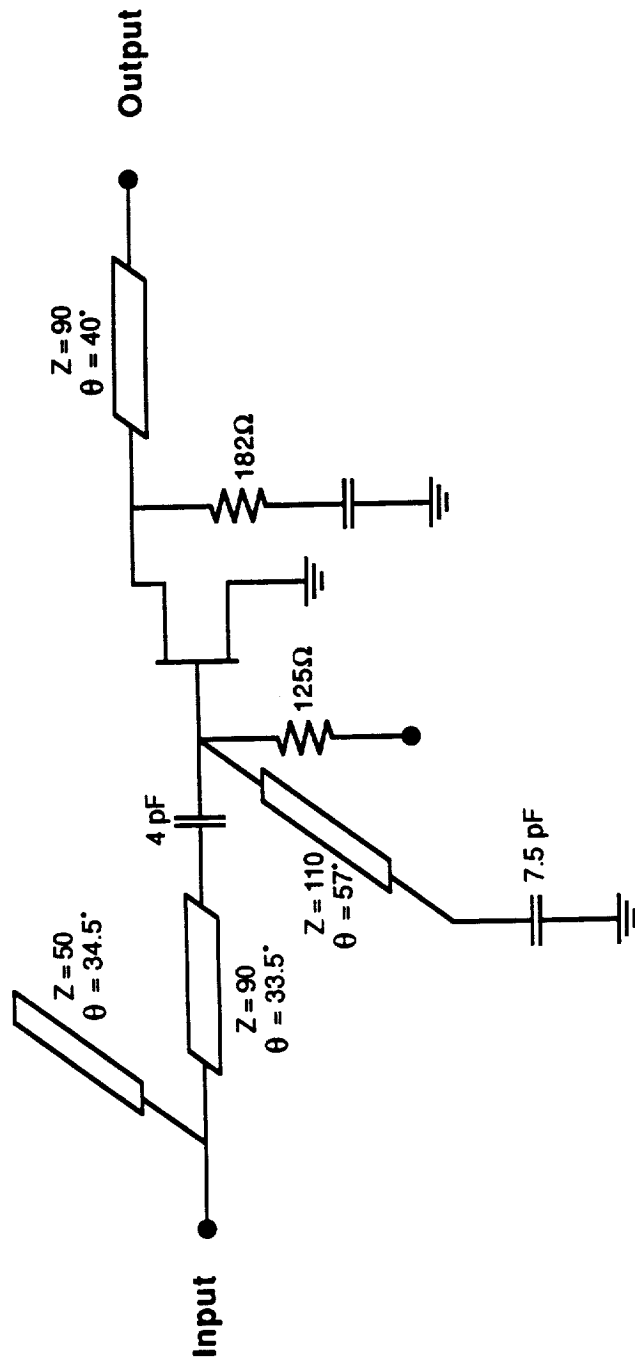


FIGURE 33. CONVERSION LOSS VS. LO DRIVE CALCULATED BY ADDING 3 DB TO LOSS MEASURED USING NOISE



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Figure 34. IF Amplifier Schematic Diagrams (0.5 micron x 300 micron FET, Reference Frequency 8 GHz).

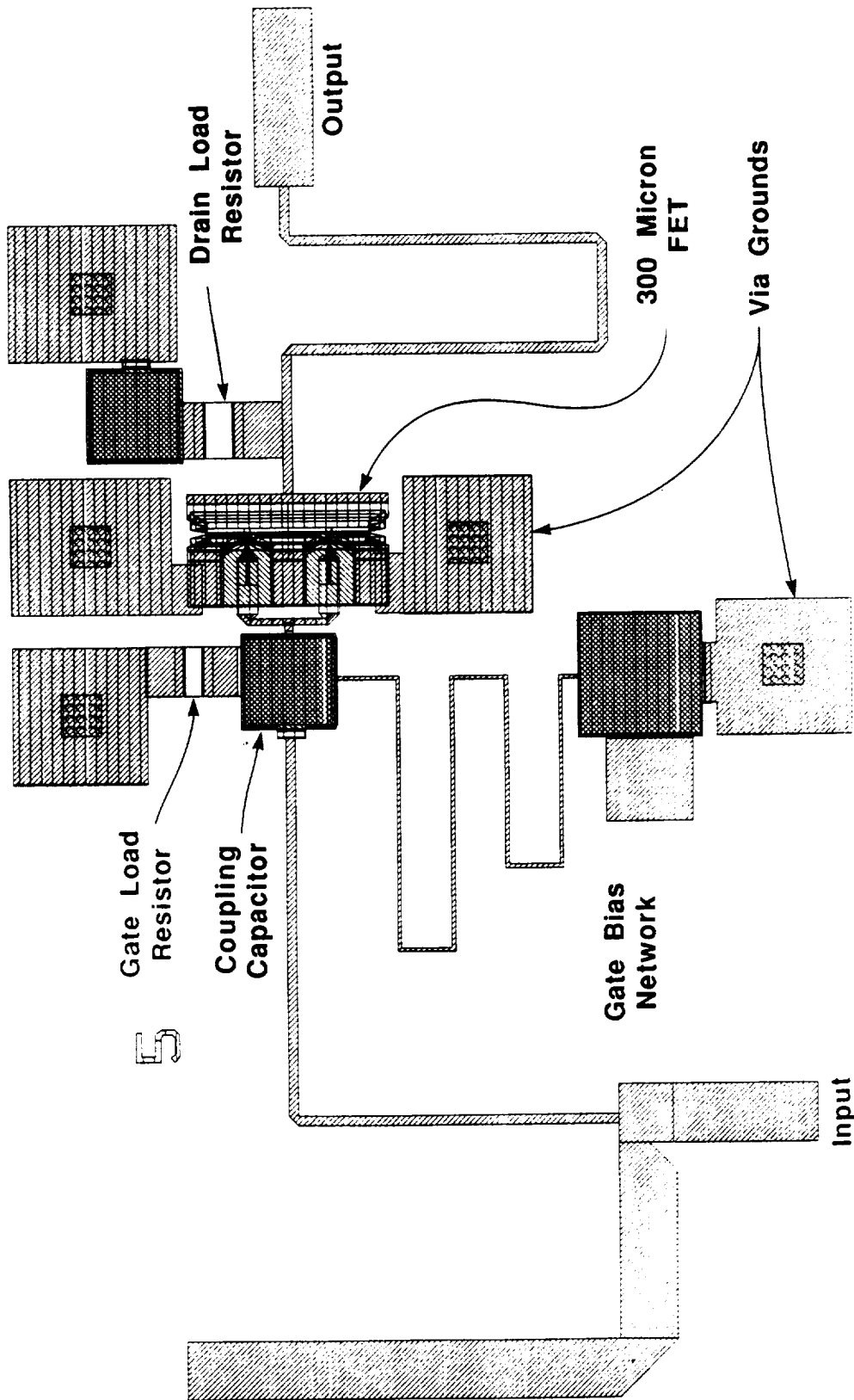


Figure 35. IF Amplifier Layout Showing Circuit Elements.

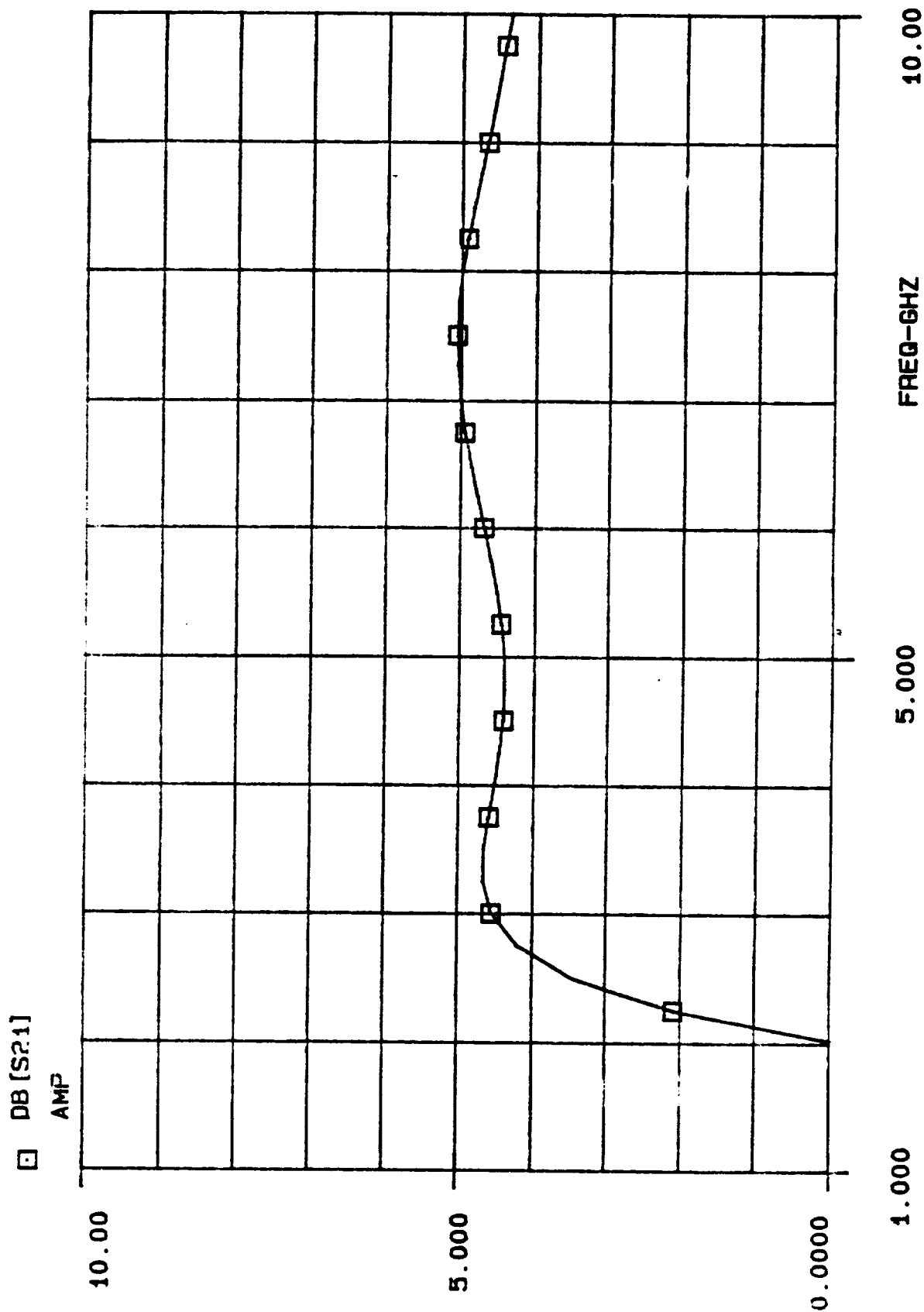


Figure 36. Calculated IF Amplifier Frequency Response Showing Mode Bandwidth.

Other mixers reported in the literature with high IF frequencies have used a mixture of transmission media. They require relatively large complex transitions for single chip circuit implementations. High diode cutoff frequencies have previously been demonstrated only with epitaxial structures. Integrating diodes using such layers with three terminal devices is a very difficult, complex process while the ion implanted approach used here is quite simple.

2.4 IF Amplifier Design

Since substantial gain in the IF amplifier is not required a single stage is used, primarily as a buffer between the mixer and external circuits. The schematic and layout of the circuit are given in Figures 34 and 35, respectively. The calculated frequency response is in Figure 36. The latter includes the effect of all of the mixer filters and indicates that the IF frequency response is suitable for this program.

2.5 22 GHz LO Amplifier Design and Performance

The 22 GHz LO amplifier design was developed and a CALMA layout generated in 1985. The design is described in the third annual report. In 1986 we completed fabrication of the LO buffer amplifier. A photo-micrograph of the completed chip, which measures $2.3 \times 0.8 \times 0.015 \text{ mm}^3$ is shown in Figure 37. The chip contains three 0.25×100 micron gate FET amplifier stages and on chip bias filters. Figure 38 shows the gain versus frequency characteristic for the chip tested. A maximum gain of about 16 dB (including fixture losses) is obtained at 22 GHz. The amplifier test fixture uses two coaxial "K-connectors" at input and output.

2.6 Status and Plans

All RF/IF wafers have been processed. The mixer diode DC characteristics are outstanding for ion implanted devices. Packaging and final RF testing of a mixer from these wafers is in progress. A total of 49 mixer ICs have been visually inspected, dc tested, and set aside for delivery. None of the IF amplifiers were fabricated with the mixer due to processing problems. We

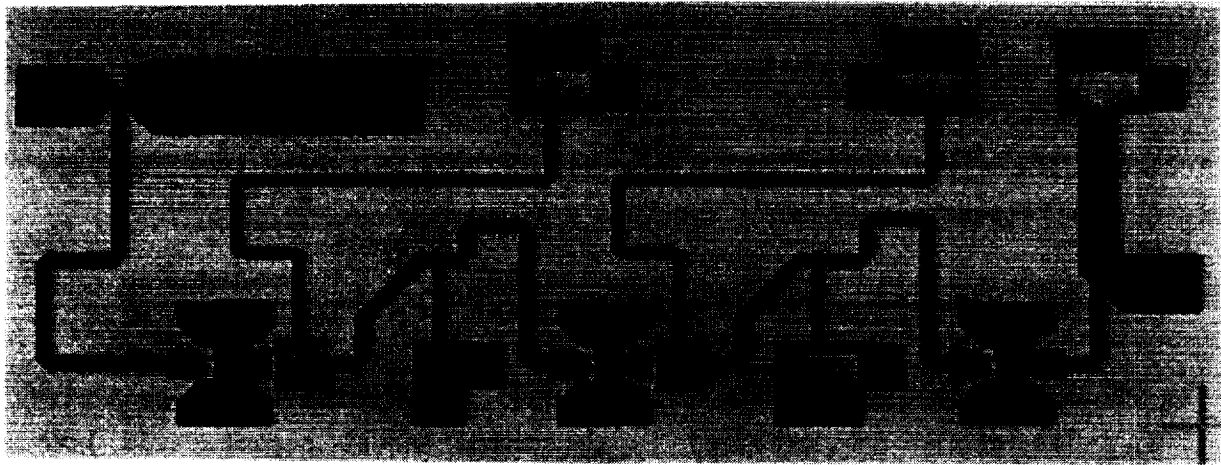
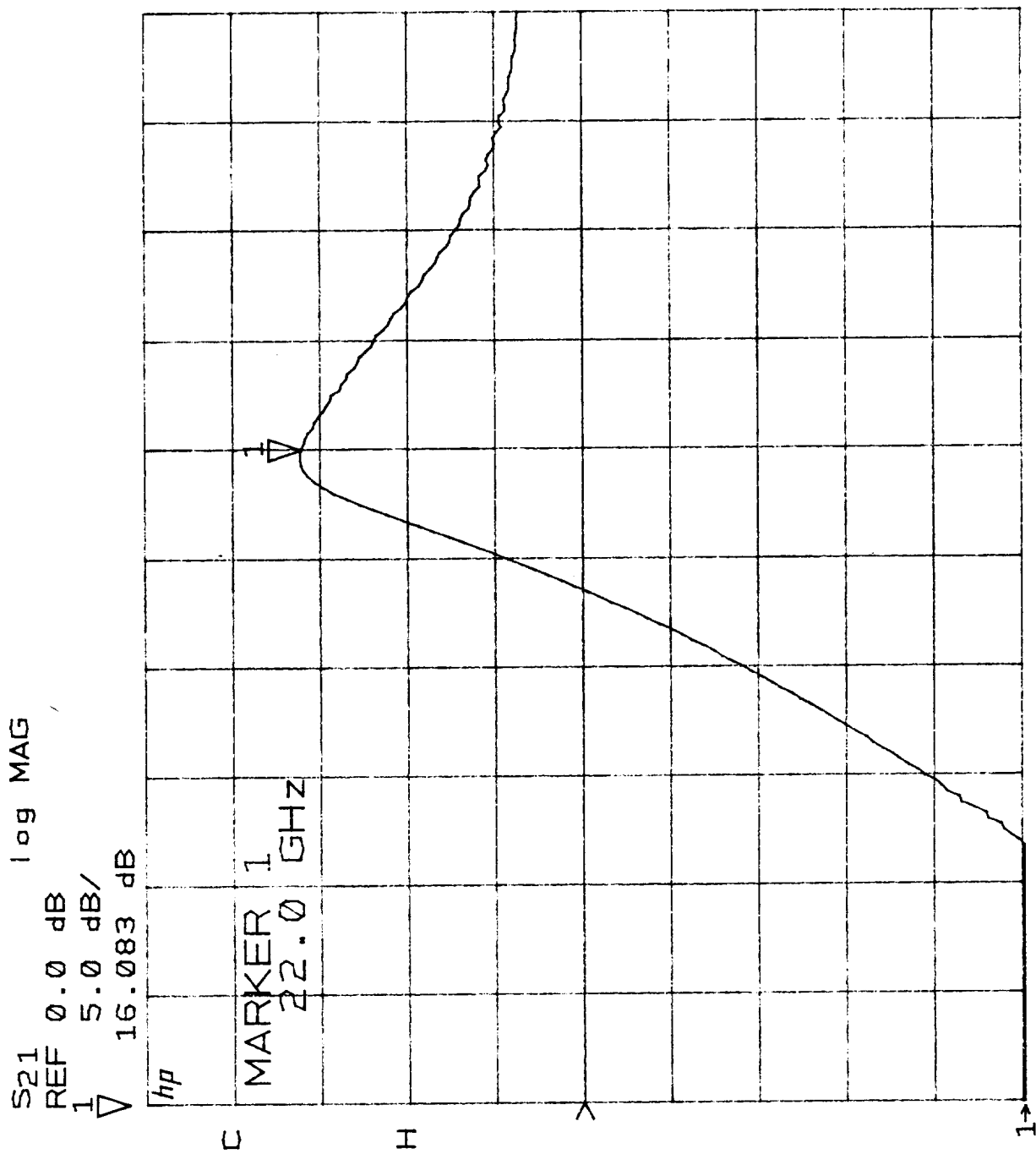


Figure 37. Photomicrograph of LO Buffer Amplifier Incorporating Three Stages of 0.25 x 100 Micron Gate Ion-Implanted FETs.



START 16.000000000 GHz
 STOP 26.000000000 GHz

Figure 38. Gain vs Frequency Characteristic for 3-Stage 22 GHz LO Buffer Amplifier.

believe these processing problems have now been solved through work on the CTS receivers. However, no additional RF/IF wafers will be processed due to funding limitations. The 49 mixer ICs plus packaged mixer will be delivered to NASA in the first half of 1988.

3.0 SUBMODULE INTEGRATION AND RECEIVE MODULE DEVELOPMENT - TASKS VI AND VII

The objectives of Tasks VI and VII are to demonstrate an interconnected receiver (using the four submodule chips) and a totally monolithic receiver, respectively. Obviously, the initiation of Task VII implies the completion or near completion of Task VI. Originally, the interconnected receiver, Task VI, was to have been completed by the forty-second month of the program, and at the end of the thirty-sixth month, three out of the four submodules (phase shifter, gain control, and RF/IF submodules) were to have been demonstrated and samples (100 of each) delivered. Although much progress had been made, only three of the submodules (a two-stage LNA, a two-stage gain control amplifier, and a 5-Bit phase shifter) were ready for interconnection towards the end of the fourth year.

As a result of this slower than anticipated sub-module development, Honeywell recommended early in the third year a program re-direction to emphasize the development of the various sub-modules and to concentrate on the demonstration of the interconnected receiver (Task VI) by the end of the fourth year of the program. With NASA's approval this action was taken and it was agreed that Task VII will be postponed to a later date in the 30 GHz receiver program.

3.1 Interconnected Receive Module Design/Preliminary Realization

The submodule performance goals as well as the overall performance goals of the interconnected receiver are summarized in Figure 39.

3.1.1 Design

Four monolithic chips constitute the interconnected receiver, the low noise amplifier, phase shifter, gain control amplifier and the RF to IF down-converter.

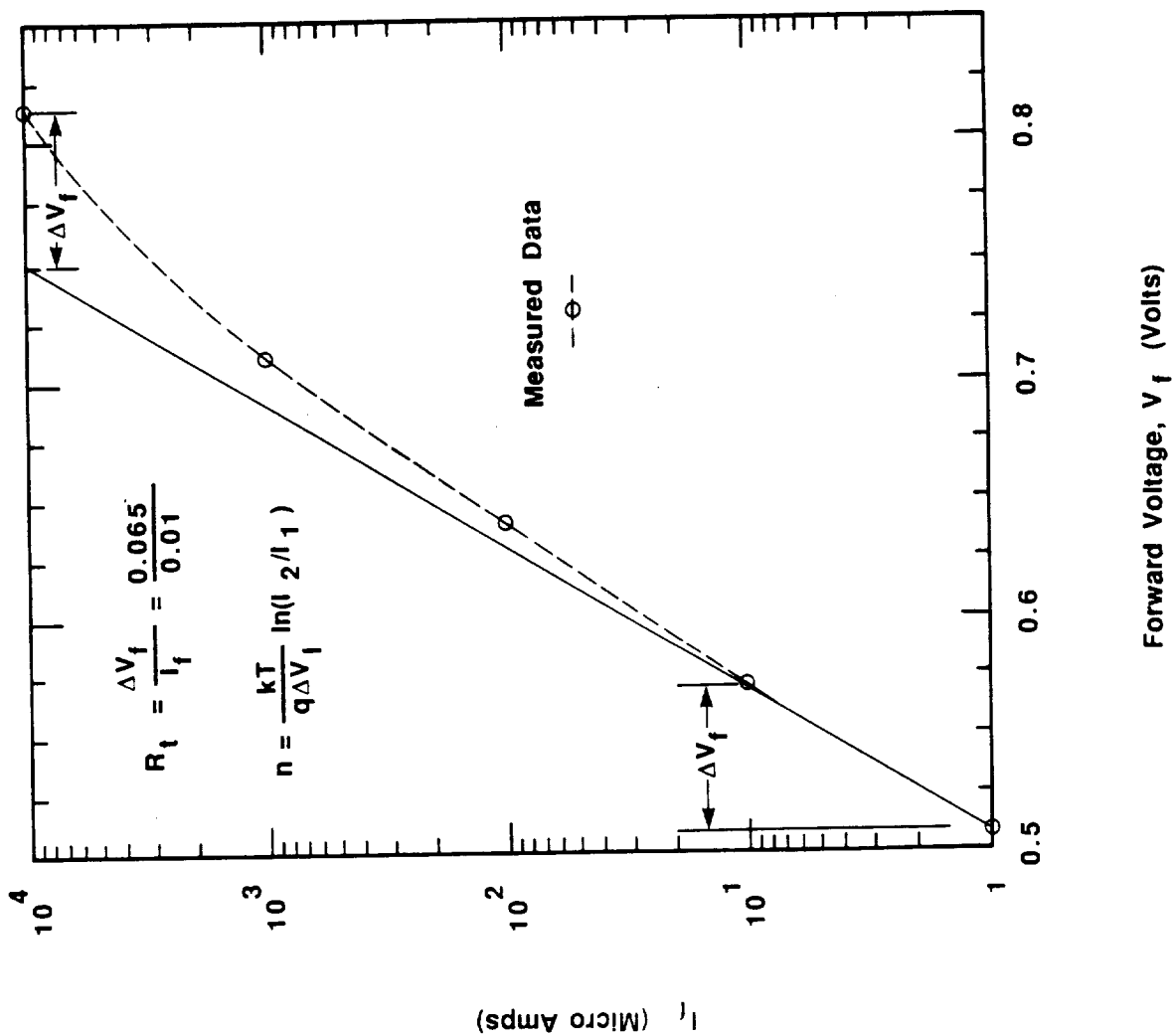


Figure 27. Measured Forward I-V Characteristic of Ion Implanted Mixer Diode.

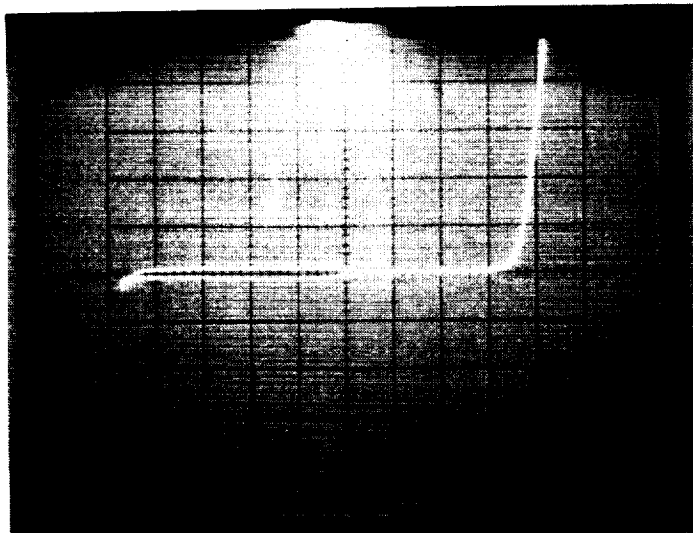


Figure 28. I-V Characteristic of Ion Implanted Diode.
Forward H: 0.2 v/div V: 1 mA/div Reverse
H: 1 v/div V: 1 μ A/div.

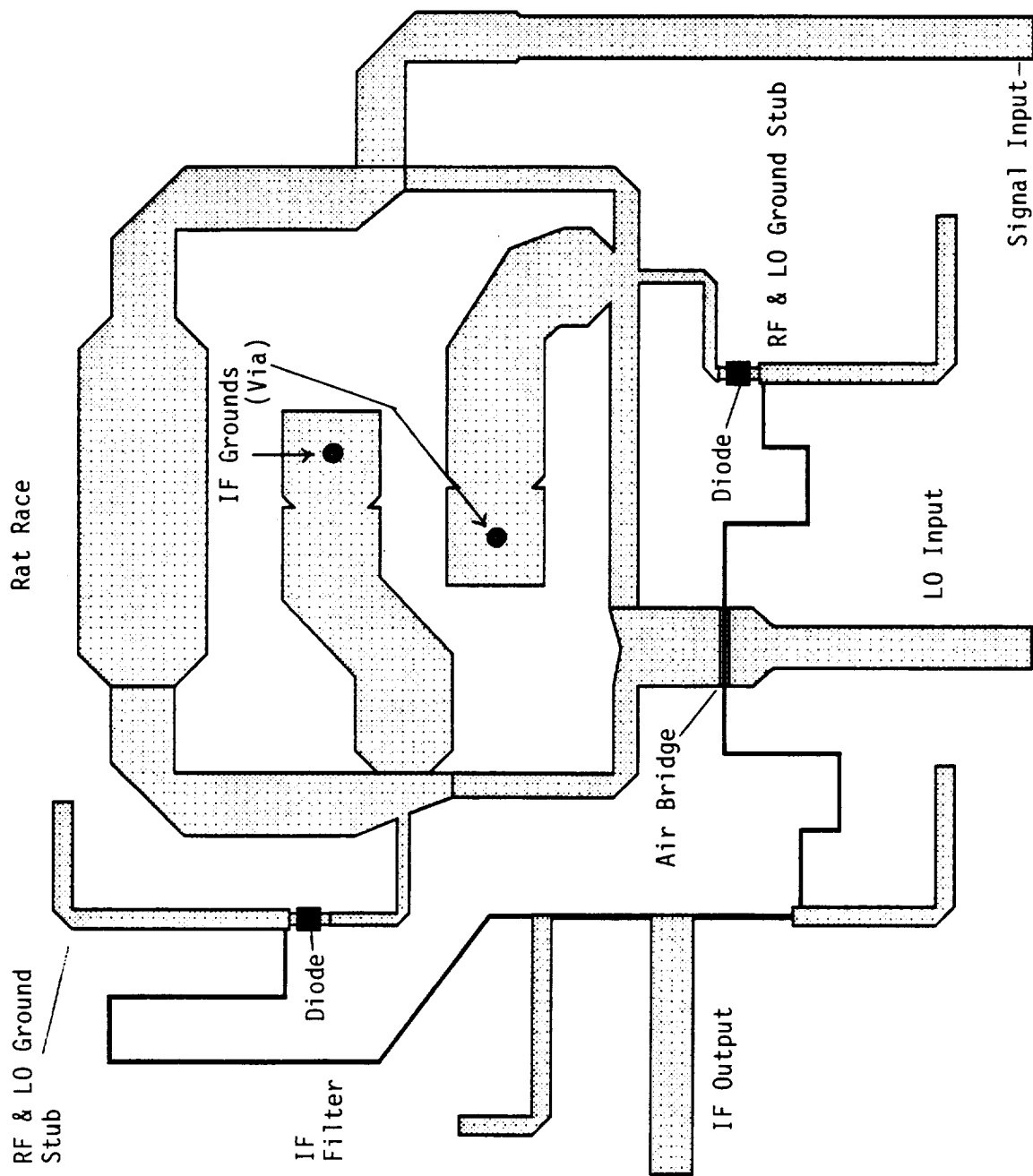


Figure 29. Mixer Layout for 115 ohm Junction Resistance.

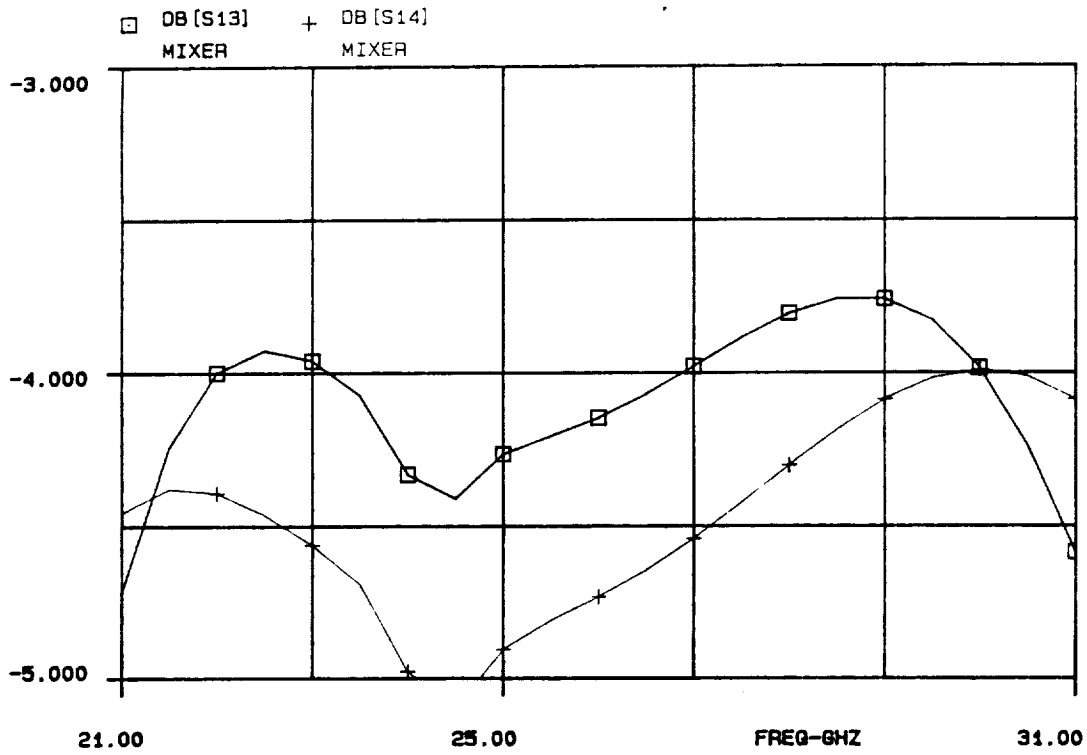
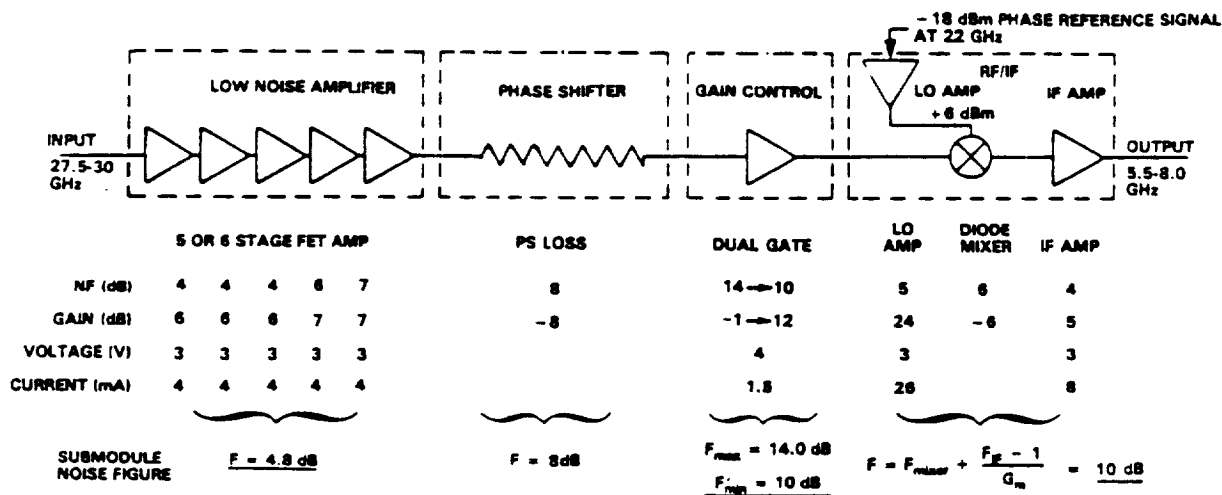


Figure 30. Signal Port Insertion Losses to 300 ohm Diode Junctions in Design 2.



Overall Performance

Noise Figure: 4.9 dB (Max Gain); 5.0 (Min Gain)
 RF/IF Conversion Gain: 35 dB (max Gain); 23 dB (Min Gain)
 Minimum Detectable Signal: -70 dBm
 Dynamic Range: 30 dB minimum

Figure 39. Goal for Inter-Connected Receiver

The receiver conversion gain is around 30 dB (depending on the gain control amplifier setting), and the overall noise figure is 5.0 dB. The gain control amplifier has adjustable gain (continuous control) over at least the -1 to +12 dB range. A 5-bit phase shifter incorporating switched line phase shifters as well as a loaded line type, is used for phase control. Note that the noise figure of the receiver is essentially set by the low noise (~ 4.8 dB), high gain (~30 dB) front-end amplifier. Frequency down conversion from the 27.5-30 GHz band to the 5.5 - 8 GHz IF is achieved in the RF/IF chip. It incorporates a balanced mixer using a pair of Schottky barrier mixer diodes, a single stage IF buffer amplifier and a local oscillator buffer amplifier.

3.1.2 Preliminary Receiver Realization

To demonstrate the 30 GHz receiver with existing ICs, a preliminary version of the receiver was assembled and demonstrated. Three monolithic chips, a two-stage LNA, a two-stage gain control amplifier and the phase shifter were assembled and tested. Prior to their interconnection, however, all three chips were individually tested to check for basic functionality and to eliminate any RF-bad ICs. Data taken on these chips is presented in Appendix A. It should be noted that the phase shifter and the gain control amplifier described in Appendix A are the actual chips used in the receiver. However, the two stage LNA in Appendix A, failed during initial testing of the interconnected receiver and a substitute LNA chip (from the same wafer) was used instead. Consequently, the data given for the LNA in the Appendix should be considered representative of the actual LNA employed in the receiver. Furthermore, to achieve operation in-band both the LNA and gain control amplifiers were modified to bring their center frequency down from about 31 GHz to the required 29 GHz. These adjustments were made with the aid of the on-chip "design alternatives" and short lengths of bond wire (see Sections 1.3 and 1.5).

The chips were mounted in a single housing having standard waveguide input and output ports as shown in Figure S-5. Some simple bias filtering and dc-blocking between chips was realized on quartz hybrid circuits (seen in Figure 40). To transition from the microstrip line input and output to the corresponding waveguide ports, low loss antipodal finline transitions were

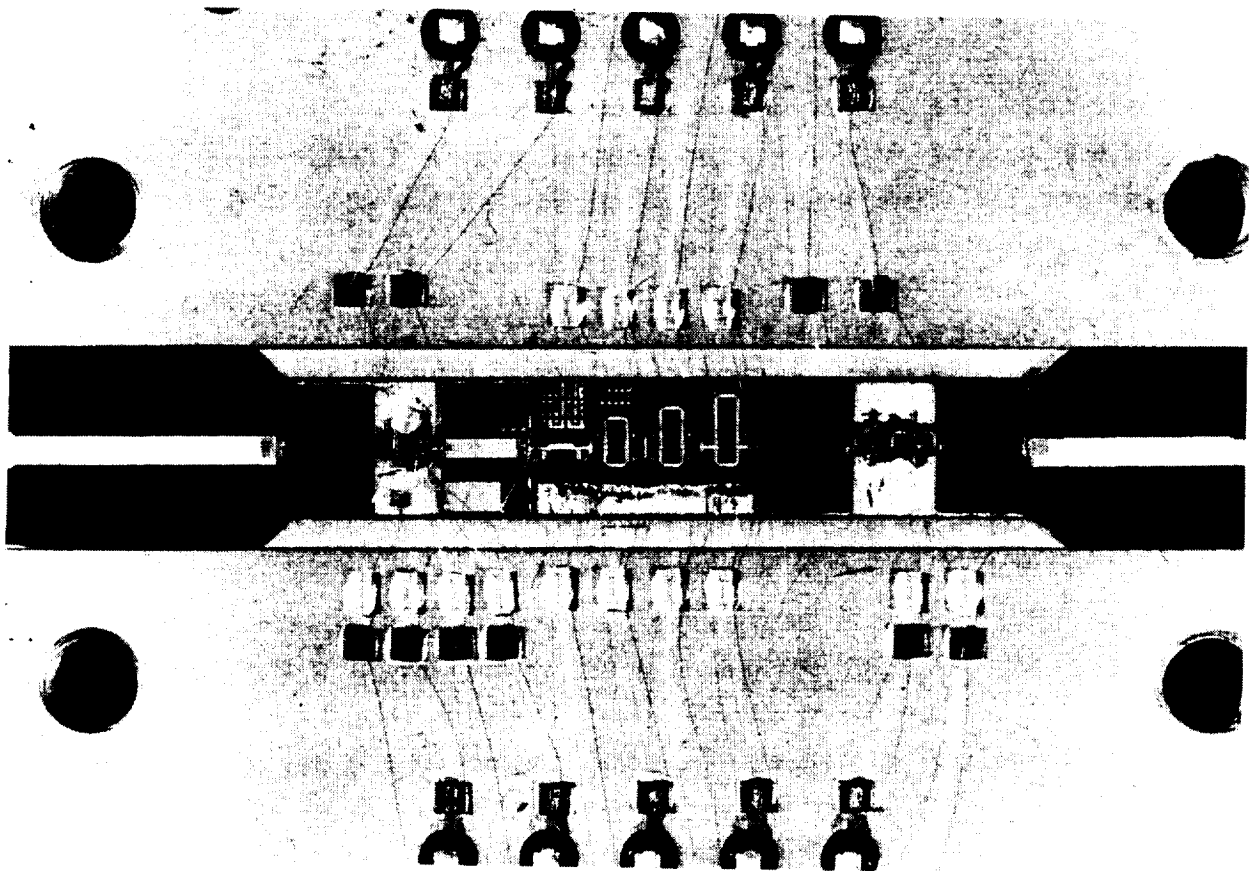


Figure 40. Close-up of Assembled Receiver.

fabricated on RT duroid and incorporated in the housing (seen in Figure S-5). For bias routing, a pair of standard 10-pin connectors and chassis feed-through holes were used. For amplifier stabilization, 1 ohm resistors in the gate bias lines were also incorporated.

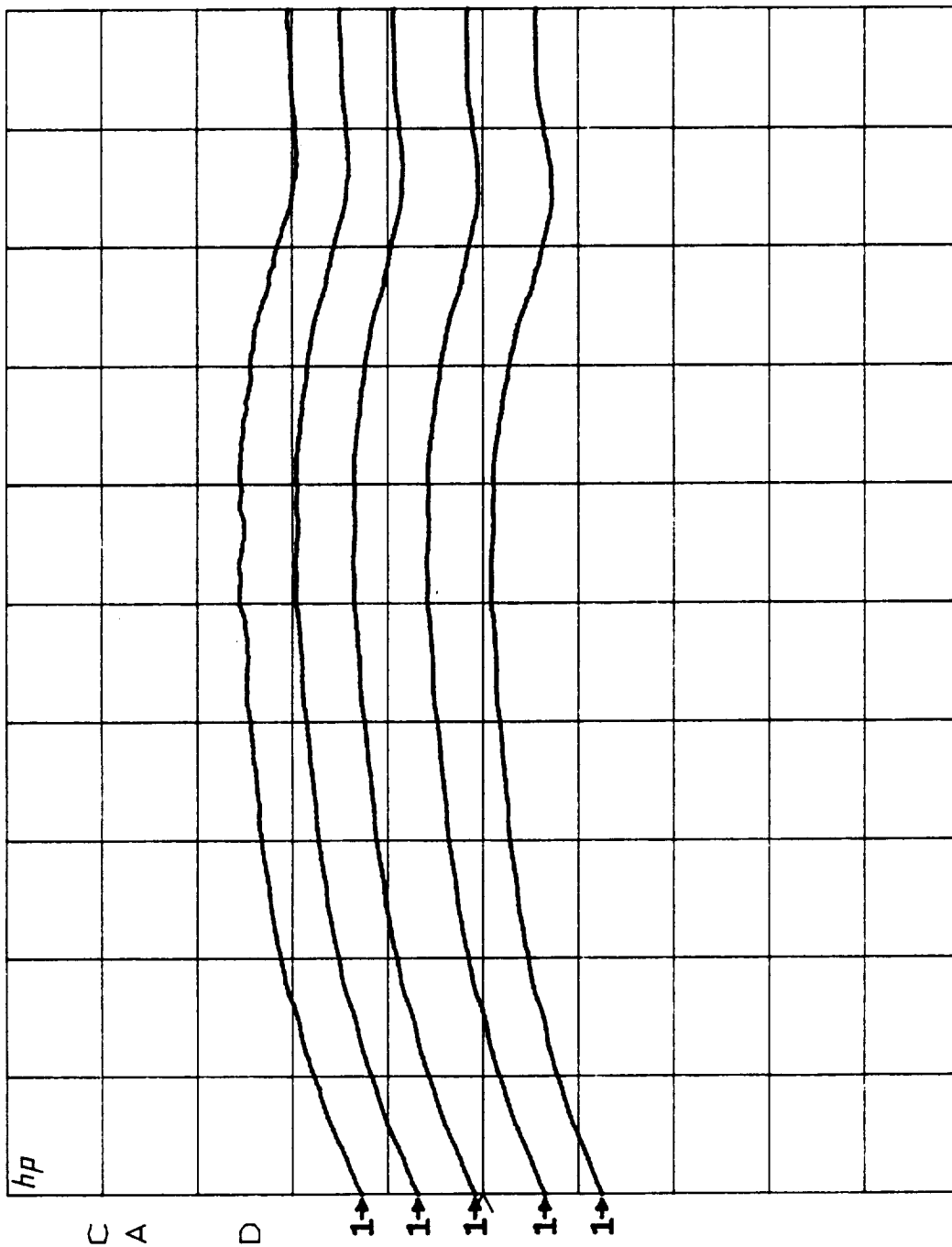
3.2 Interconnected Receive Module Performance

RF testing of the interconnected receive module (IRM) includes gain/loss measurements, relative phase shift measurements, and noise figure. Gain and phase measurements were carried out on the H.P. 8510 network analyzer system with the Ka-band system extension. A full set of measurement data was delivered to NASA at the time of actual demonstration of the receiver at the Lewis Research Center. This data is also presented in Appendix B. In this subsection we will present representative data taken on the receiver including the noise figure data. Note that in this preliminary receiver realization the gain of the two-stage low noise amplifier (LNA) is only 7 - 10 dB at the low noise bias point. For the cascaded two-submodule (CTS) receiver a six-stage 30 dB gain amplifier will be employed (currently in fabrication). Discussion of the four and six-stage designs is given in the following subsection.

Figure 41 shows the gain versus frequency characteristic for the IRM for five gain settings ($\sim +13$ dB to -1 dB) across the 27.5 - 30 GHz band. Worst case gain ripple across this 2.5 GHz band is less than ± 3 dB and is ± 1.5 dB for a reduced bandwidth of about 1.5 GHz. The main band-limiting circuit is the gain control amplifier. The corresponding relative phase shift is shown in Figure 42. Worst case phase wander for the five gain settings is approximately $\pm 12^\circ$, occurring at the band edges.

Figure 43 shows the relative insertion phase characteristics as the phase shifter chip is cycled through sixteen phase states (note that although tests were made on only 4 bit operation of the phase shifter, the fifth bit was functional since the fourth and fifth bits are incorporated into the same loaded line phase shifter segment). Nearly full 360° coverage is obtained at the upper band edge, while reduced coverage of about $310 - 320^\circ$ is achieved in the lower half of the band. Nominally, for 360° coverage at center frequency (28.75 GHz), approximately 345° and 375° coverage should be obtained at the lower (27.5 GHz) and upper (30 GHz) band edges respectively, for true time

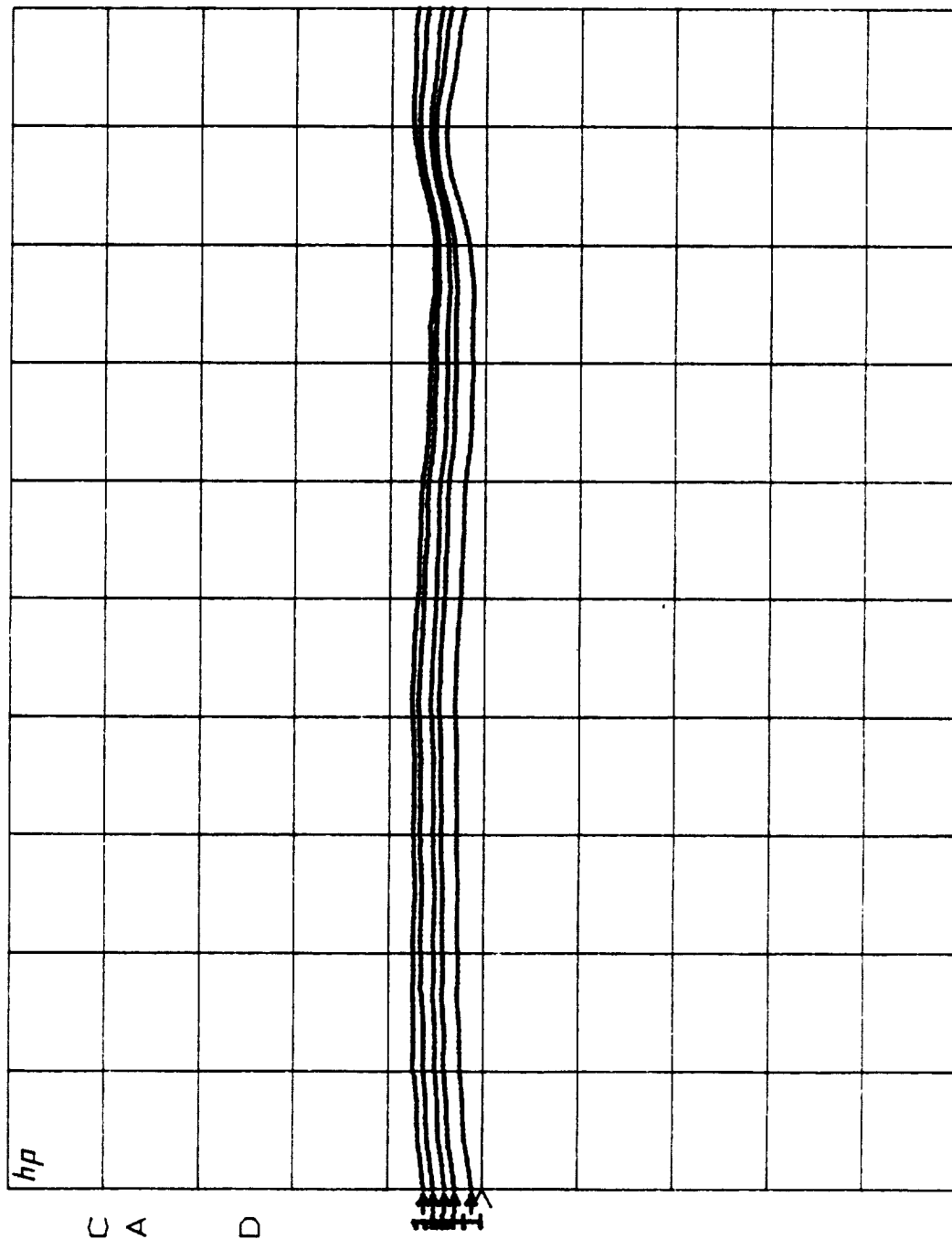
S21 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure 41. Receiver Gain Characteristics

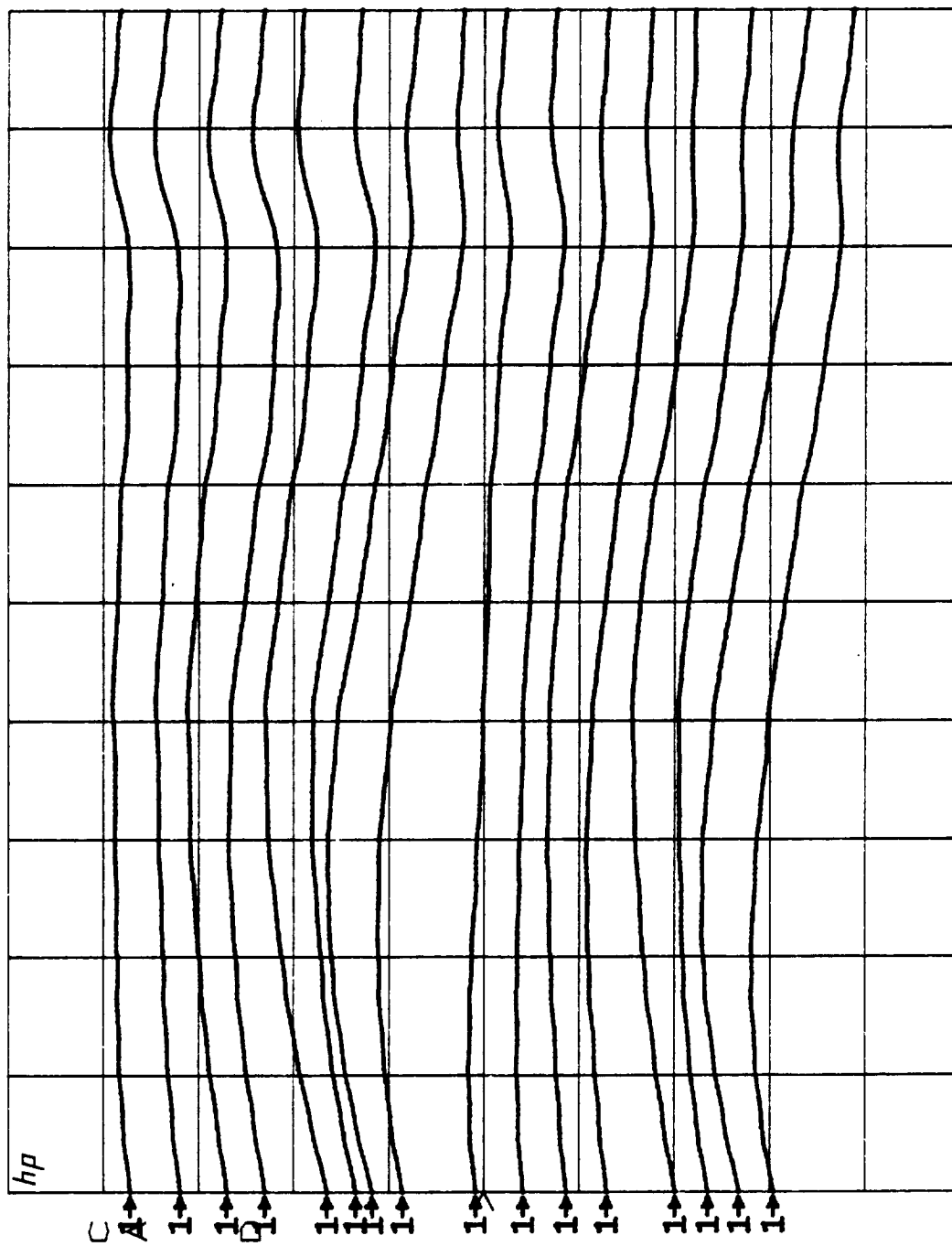
S21 \angle
 REF 0.0 °
 45.0 °/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure 42. Receiver Insertion Phase vs. Gain Adjustment.

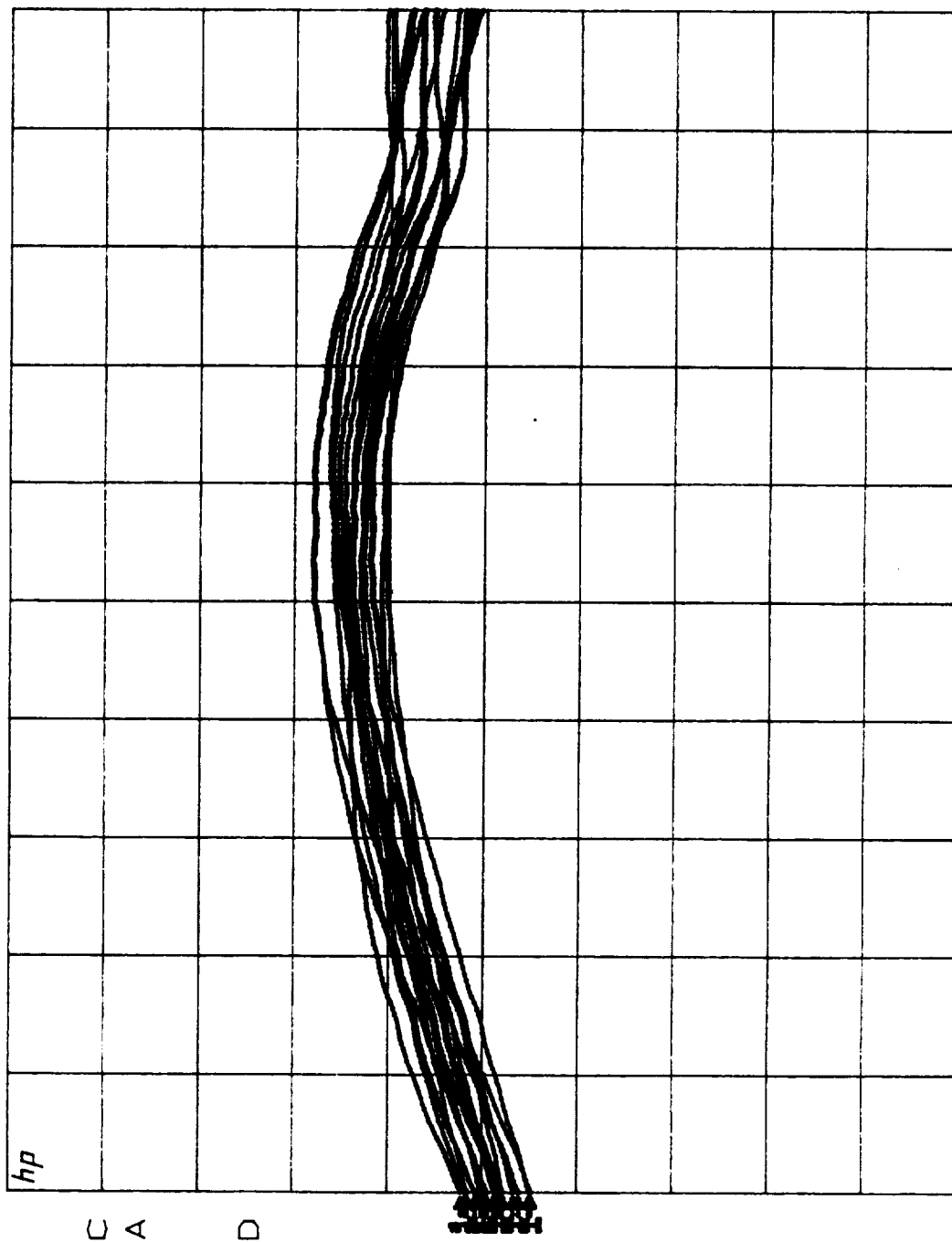
S21 \angle
 REF 0.0 °
 45.0 ° /



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure 43. Receiver Relative Phase States.

S21 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure 44. Receiver Gain Variation During Phase Adjustments.

delay 4-bit phase shifters. Note these phase characteristics are similar to those measured on the individual phase shifter chip. Finally, Figure 44 shows the gain wander as the phase shifter is cycled through the sixteen phase states. As seen in the figure, the total gain variation is about ± 2 dB and is fairly constant across the band of interest.

Noise figure data was taken at center band for the nominal gain settings of +12, 9, 6, 2 and -1 dB. Table 2 shows the resultant data. Best noise figure of 14 dB was obtained at the highest gain setting. It is important to realize that the relatively high noise figure data is a direct consequence of insufficient front-end gain. This can be shown to be the case by calculating the receiver noise figure given the noise figure of the individual modules using Friis' formula. Thus if we take the following submodule data:

LNA:	Gain = 10 dB	N.F. = 7 dB
Phase Shifter:	Loss = 8 dB	N.F. = 8 dB
Gain Control Amplifier:	Gain = 12 dB	N.F. = 16 dB

and apply Friis' formula to a cascade of three amplifiers having these gain and noise figure values, the resultant overall receiver noise figure becomes 14.8 dB. This value agrees well with the measured noise figure data in Table 2 for the maximum gain setting. Furthermore, if values of -1 dB and 19.7 dB for the gain and noise figure respectively of the GCA at minimum gain are used (actual measured values on GCA), the resultant overall receiver noise figure (leaving the other submodule gain and noise figure values unchanged) becomes 18.0 dB, which again agrees well with the corresponding measured receiver noise figure at minimum gain (-1 dB).

To achieve receiver noise figures of less than 6 dB, a high gain (~ 30 dB) front-end amplifier with a noise figure of around 5 dB is required. Such LNA's are currently being fabricated.

As mentioned earlier, delivery of the first three-submodule receiver was accomplished at the end of the fourth program year. Two additional receivers of the same type were delivered early in the fifth year. A paper describing some of these results was presented at the 1987 GaAs IC Symposium [4].

TABLE 2

RECEIVER NOISE FIGURE DATA

f = 28.75 GHz

GAIN SETTING	NOISE FIGURE
"12 dB"	14.0 dB
" 9 dB"	14.8 dB
" 6 dB"	15.7 dB
" 2 dB"	17.2 dB
"-1 dB"	18.5 dB

Delivery of the RF/IF submodule is expected in the first half of 1988. The RF/IF chip is housed in a separate housing having waveguide input and coax output ports. For antenna feed array applications, it has been shown that it is advantageous to realize the beam forming network at RF [Ref 1]. Consequently, the RF/IF chip is not physically located or housed in close proximity to the three front-end submodules. Therefore, the four-submodule interconnected receiver, to be demonstrated in the fifth year, will consist of two housings bolted together. The second housing containing the RF/IF submodule will also be used for the cascaded two-submodule (CTS) receiver discussed in the following subsection.

3.3 CTS Receiver Development

The goal for the CTS receiver is to monolithically integrate the front-end RF submodules, namely the LNA, phase shifter, and the GCA. To accomplish this on a single chip, it was determined that the phase shifter layout would have to be significantly reduced in size. Furthermore, a five or six stage LNA would have to be incorporated instead of the two stage LNA.

As an initial step towards achieving these goals a mask set was generated that included the following designs:

- o A reduced size 5-bit phase shifter
- o A two-stage LNA
- o Digital control circuits
- o Four and six-stage LNAs
- o Test FETs and circuits

The first three items above are a combined layout representing a single monolithic IC, while the last two items are included as separate ICs. Figure 45 shows the reticle layout for this mask set.

5002-A-0000

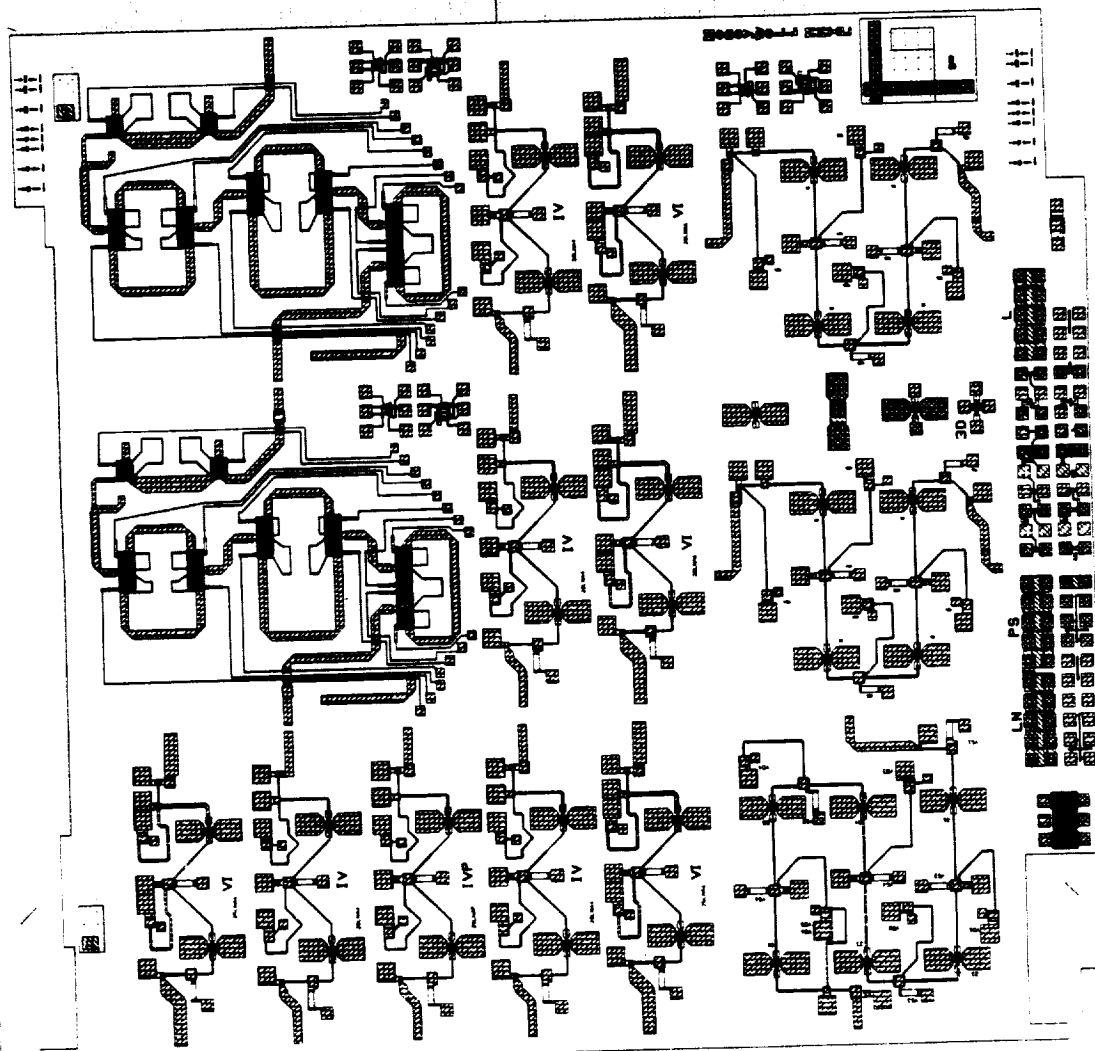


Figure 45. Reticle Layout for CTS Receiver.

The low noise amplifier designs for the CTS receiver were based on a 0.25 X 100 micron single gate FET equivalent circuit. Figure 17 shows the equivalent circuit model that was derived from measured S-parameters (DG43). The first design was reported in June 1986, and was based on a 6-mil thick substrate. Due to thickness constraints imposed by the via hole process, as well as the need for a compact phase shifter layout, subsequent designs were based on a 4-mil substrate. Consequently, all the designs on the mask set in Figure 45, except for one six-stage LNA, are based on a 4-mil thick substrate.

Figure 46 shows the Touchstone^R computer program listing for the two-stage design while Figure 47 shows the corresponding circuit schematic. Note that we have used three circuit blocks, INPUT, OUTPUT, and AMP2. The AMP2 block is used in cascade with itself to achieve the four and six stage amplifier designs. This cascaded approach also simplifies construction of the computer generated layouts. The calculated gain vs. frequency characteristics for the two, four, and six-stage designs are shown in Figures 48, 49, and 50, respectively. Although the predicted gain ripple is ± 2 dB for the six-stage design, it is expected that in the actual realization bias adjustment of the individual stages will help reduce the ripple (in the calculated amplifier it is assumed that all stages are biased identically at the low noise bias point, $\sim 0.5 I_{DSS}$) and allow increase of the gain to better than 30 dB.

Finally, Figure 51 shows the layout of the LNA/phase shifter IC consisting of a reduced-size 5-bit phase shifter, the two-stage LNA, and the digital control circuit. Predicted performance for this IC includes 5-bit phase shifting capability at 30 GHz with 0 dB loss and digital control of the phase shifter settings.

Fabrication of the CTS MMICs began in 1987. The CTS process is more complex than processes used previously since multiple implants are necessary for the phase shifter switch FETs, logic FETs, and LNA FETs. In addition, the gate level process steps are carried out separately for each device since the gate lengths and recess etch depths are different for each device.

The CTS receiver fabrication uses a hybrid lithography process with direct-step-on-wafer (DSW) optical exposure for all levels except the LNA gate. The

Touchstone (TM) -Ver(1.40-Lot 101)-Targ(IBM-PC/AT)-Ser(16002-1951- 1000)
 2SCTC.CKT 11/15/86 - 13:24:13

VAR

L1#1 7.61036 20
 Z1#70 90.00000 90
 L2#4 10.71734 15
 Z2#70 90.00000 90
 L3#15 20.72100 30
 Z3#70 90.00000 90
 Z4#70 89.99998 90
 L4#10 17.58167 20
 L5#15 19.43507 25
 Z5#65 82.19402 90
 C1#.01 0.21344 .5
 C3=1.0
 C4#.2 0.39076,.5
 R1=1.OE3
 !C6#.05 0.22814 2

DIM

LNG MIL

CKT

CAP 1 20 C#.01 0.15932 1.2
 IND 20 0 L=.03
 TLINP 1 2 Z=90 L=L1 K=7.46 A=.0044 F=30
 DEF2P 1 2 INPUT

 TLINP 1 2 Z=90 L=35.17846 K=7.45 A=.0044 F=30
 CAP 2 3 C=1
 DEF2P 1 3 BIAS

 TLINP 4 5 Z=90 L=L2 K=7.46 A=.0044 F=30
 CAP 3 4 C=1
 RES 4 0 R=R1
 !IND 20 0 L=.03
 S2PA 5 6 0 LNA43S
 TLINP 6 7 Z=90 L=L3 K=7.46 A=.0044 F=30
 CAP 7 8 C=1
 TLINP 8 9 Z=90 L=L4 K=7.46 A=.0044 F=30
 CAP 7 30 C#.01 0.24260 1.2
 IND 30 0 L=.03
 BIAS 7 0
 RES 8 0 R=R1
 !IND 40 0 L=.03
 S2PA 9 10 0 LNA43S
 TLINP 10 11 Z=82.2 L=L5 K=7.61 A=.0037 F=30
 BIAS 11 0
 DEF2P 3 11 AMP2

 CAP 1 20 C#.01 0.33431 2
 IND 20 0 L=.03
 TLINP 1 2 Z=90 L#4 6.48578 10 K=7.46 A=.0044 F=30
 CAP 2 30 C#.05 0.21603 2
 IND 30 0 L=.03
 CAP 2 3 C=1
 DEF2P 1 3 OUTPUT

INPUT 1 2
 AMP2 2 3
 !AMP2 3 4
 !AMP2 4 5
 OUTPUT 3 4
 DEF2P 1 4 AMP6

FREQ
 SWEEP 25 33 .5

OUT
 AMP6 DB[S11] GR2
 AMP6 DB[S22] GR2
 AMP6 DB[S21] GR1
 AMP6 K
 AMP6 S11
 AMP6 S22

GRID
 RANGE 25 35 1
 GR1 5 15 1
 GR2 0 -20 2

OPT
 RANGE 26 32
 AMP6 DB[S21] 28
 AMP6 DB[S21] 31

70403

Figure 46. Touchstone Program Listing for 2-Stage Design.

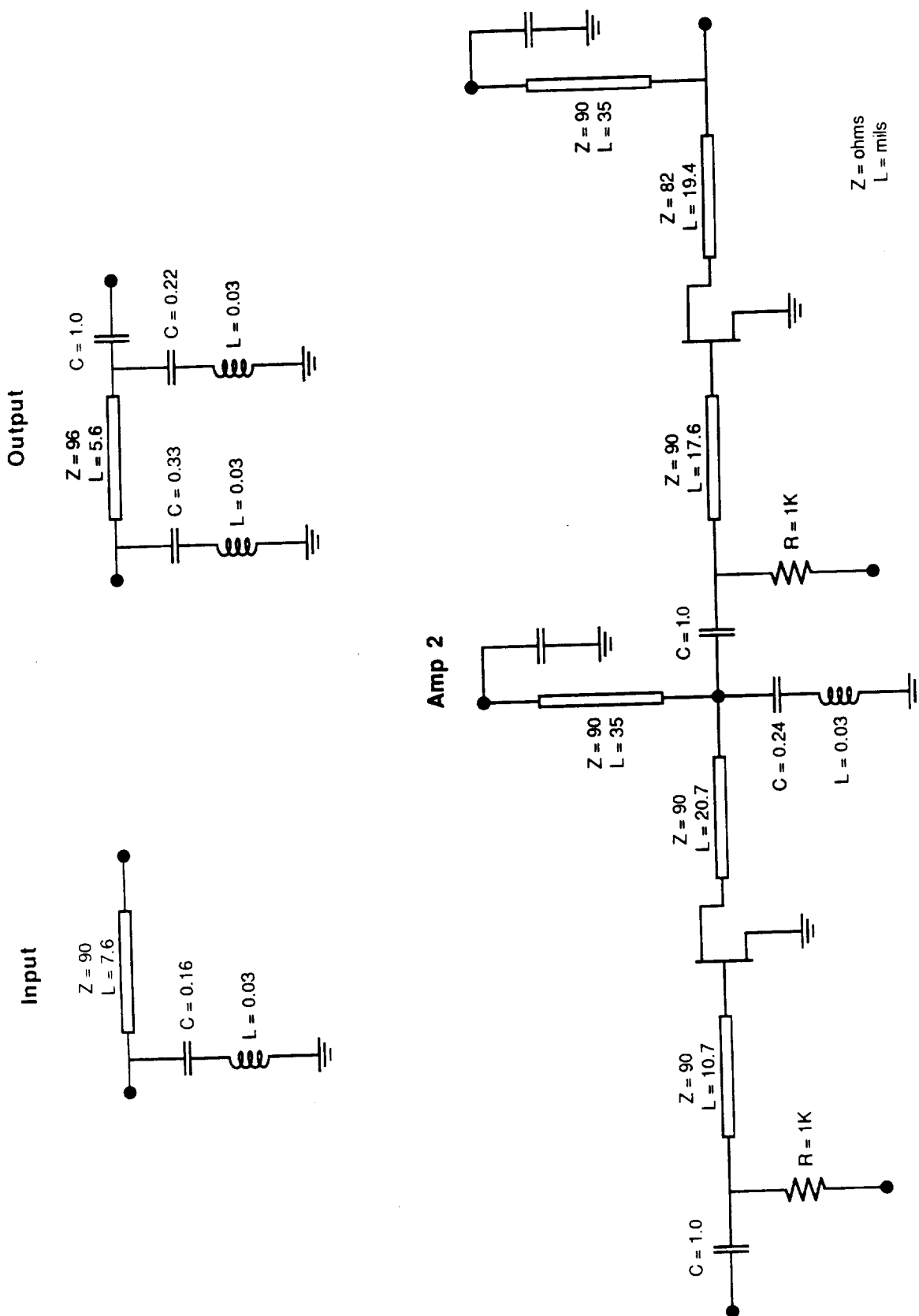


Figure 47. Circuit Schematic for INPUT, OUTPUT, and AMP2 Blocks.

EEsof - Touchstone - 01/01/80 - 01:31:51 - 2SCTC

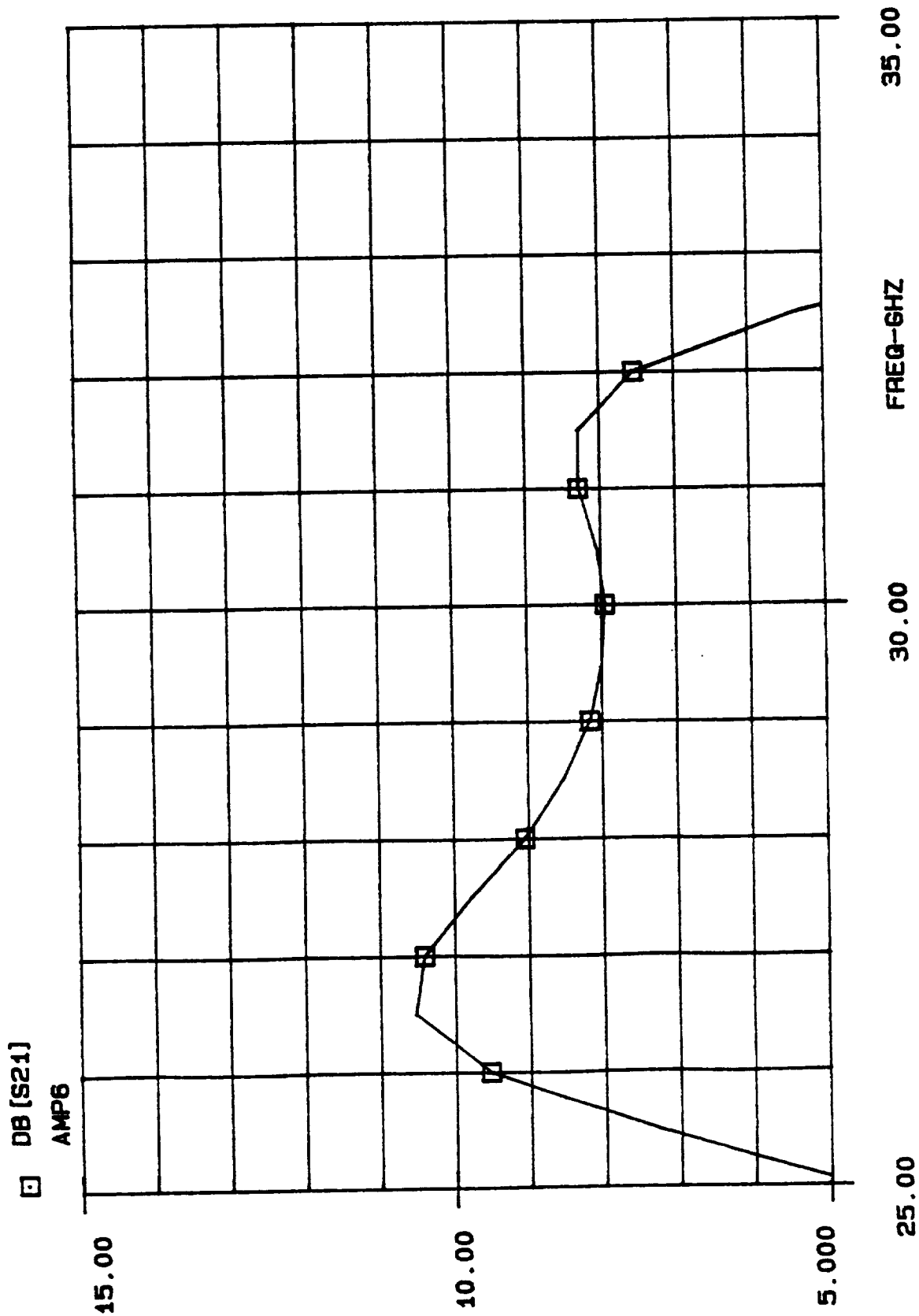


Figure 48. Calculated Two-Stage Amplifier Response.

EE801 - Touchstone - 01/01/80 - 02:30:53 - 2SCTC

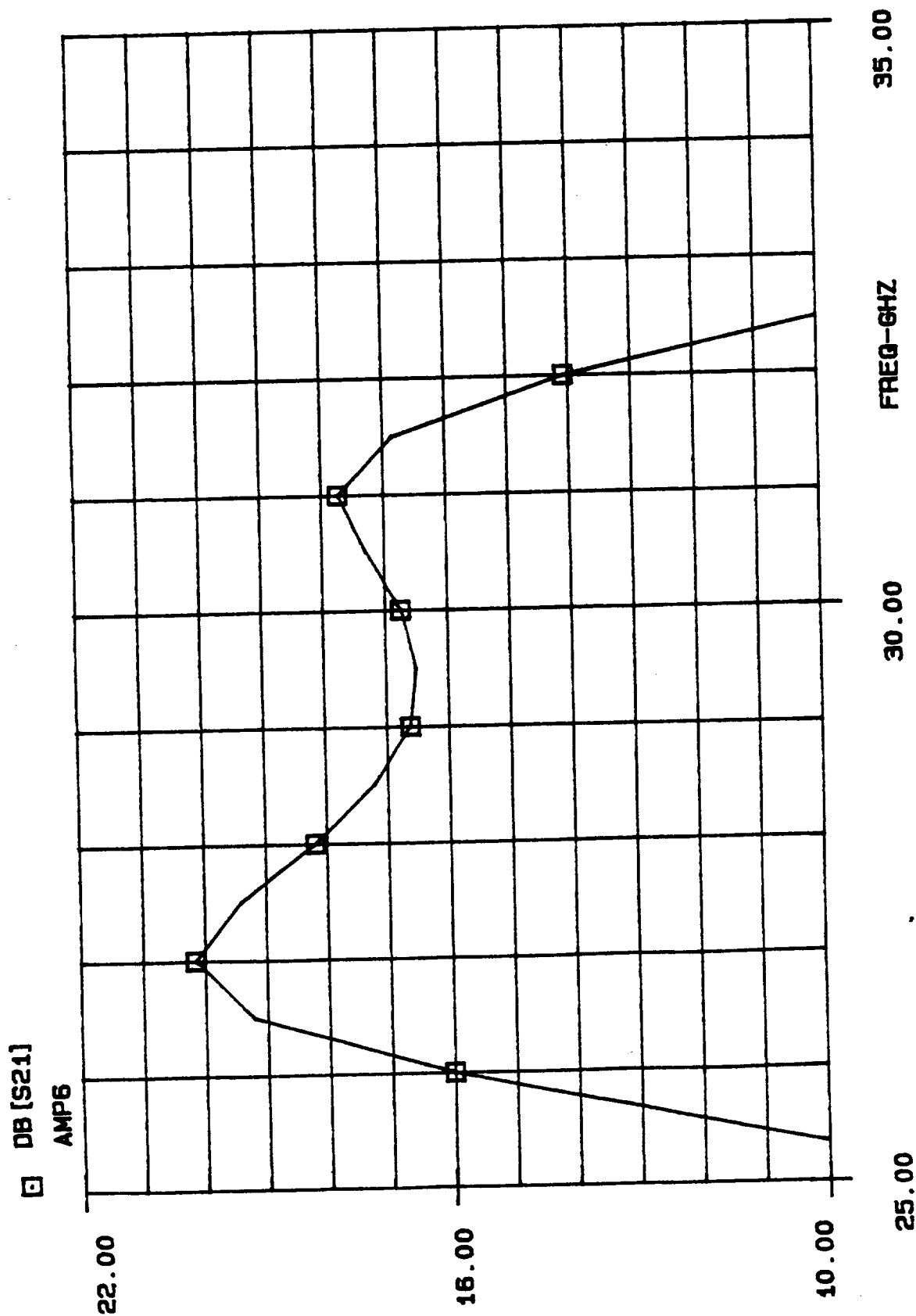


Figure 49. Calculated Four-Stage Amplifier Response.

EEsof - Touchstone - 01/01/80 - 02:39:08 - 2SCTC

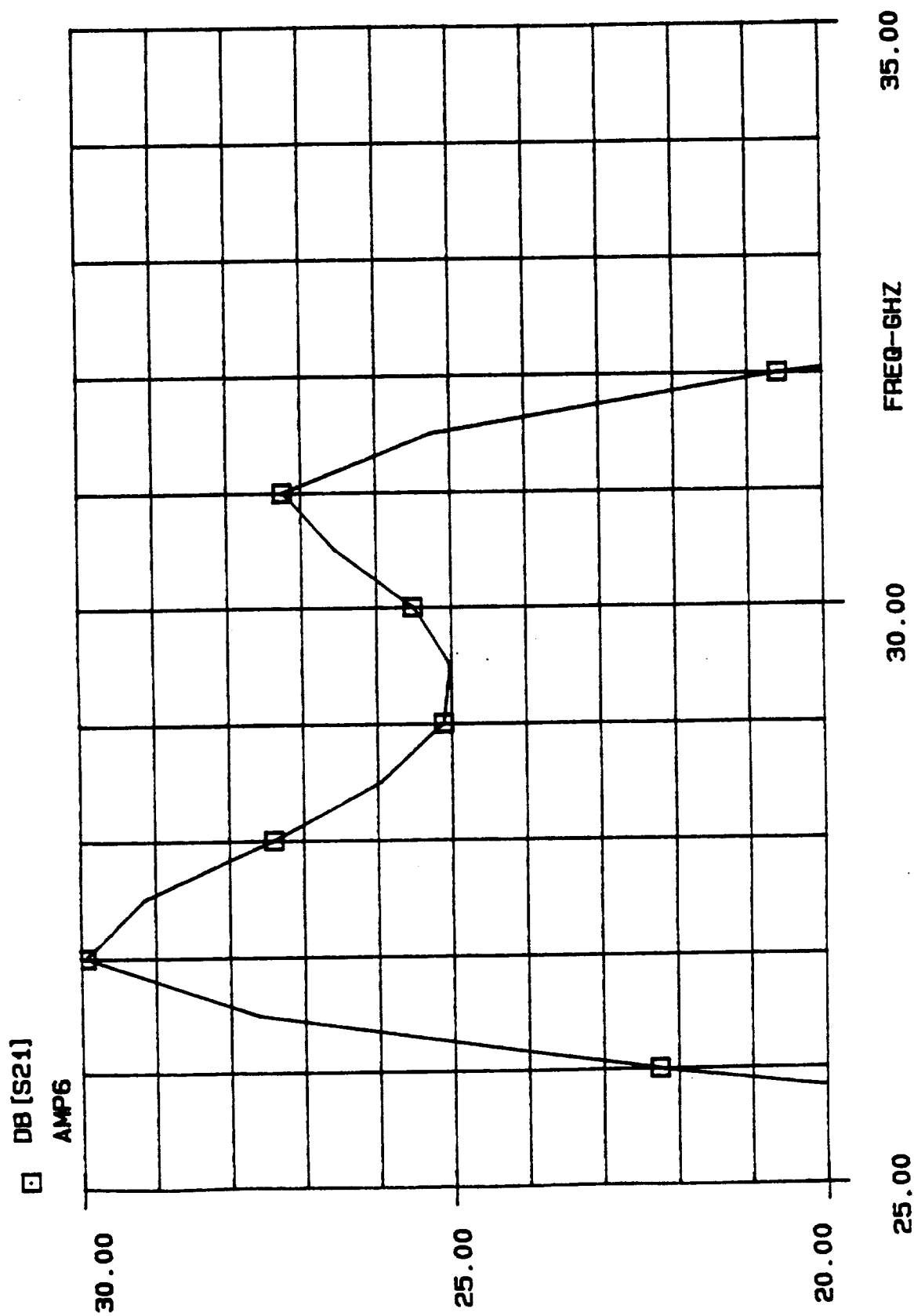
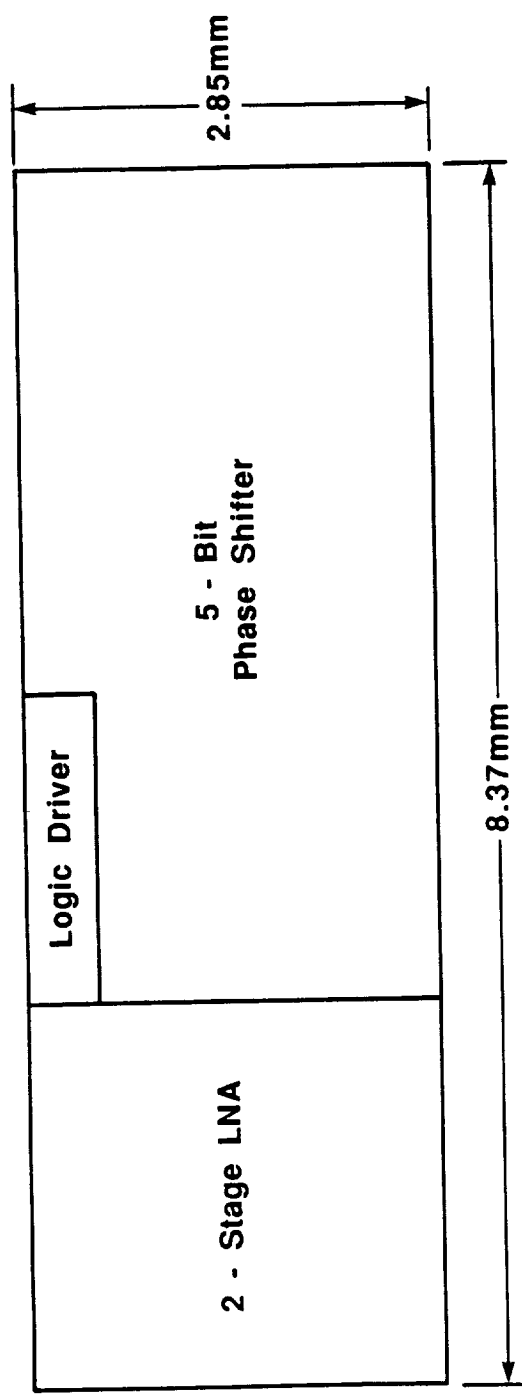
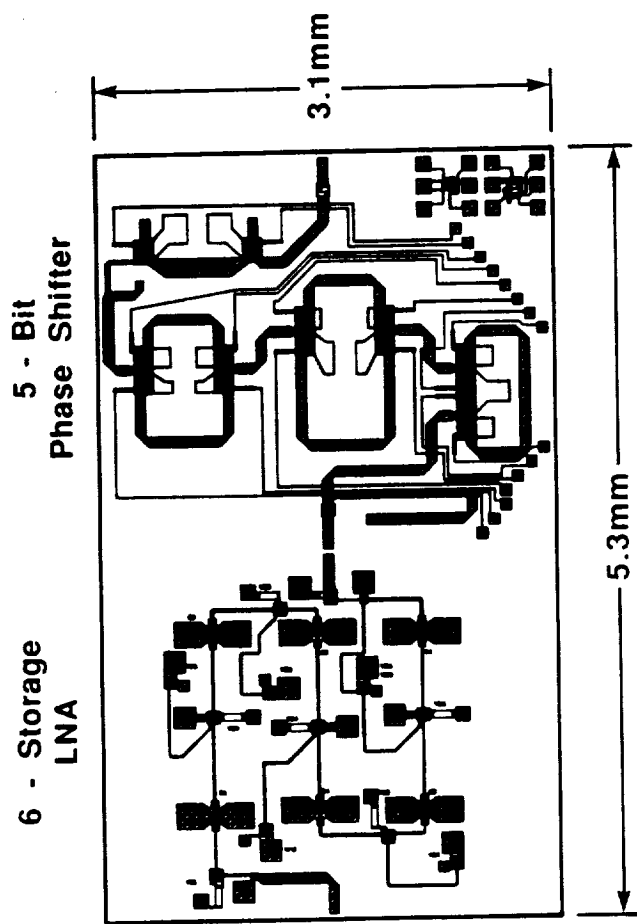


Figure 50. Calculated Six-Stage Amplifier Response.



(a)



(b)

Figure 51. LNA/Phase Shifter IC Layout.

LNA gate is exposed by E-beam direct writing in a multi-layer resist. Fabrication is done on full 3 inch wafers in contrast to earlier work which used quarters of 3 inch wafers.

The first CTS receiver wafers processed were carried through optical lithography process steps only since the E-beam system was being moved to a new location. Initial processing of the CTS wafer uncovered a number of process related problems including:

- o Error in a mask dimension - a critical mask dimension was too small to allow proper liftoff.
- o Problems associated with recess etching of the gates.
- o Poor logic FET characteristics caused by a thin layer of silicon nitride between the logic FET gate and the GaAs channel.
- o A mask error which caused shorting of a phase shifter control line.

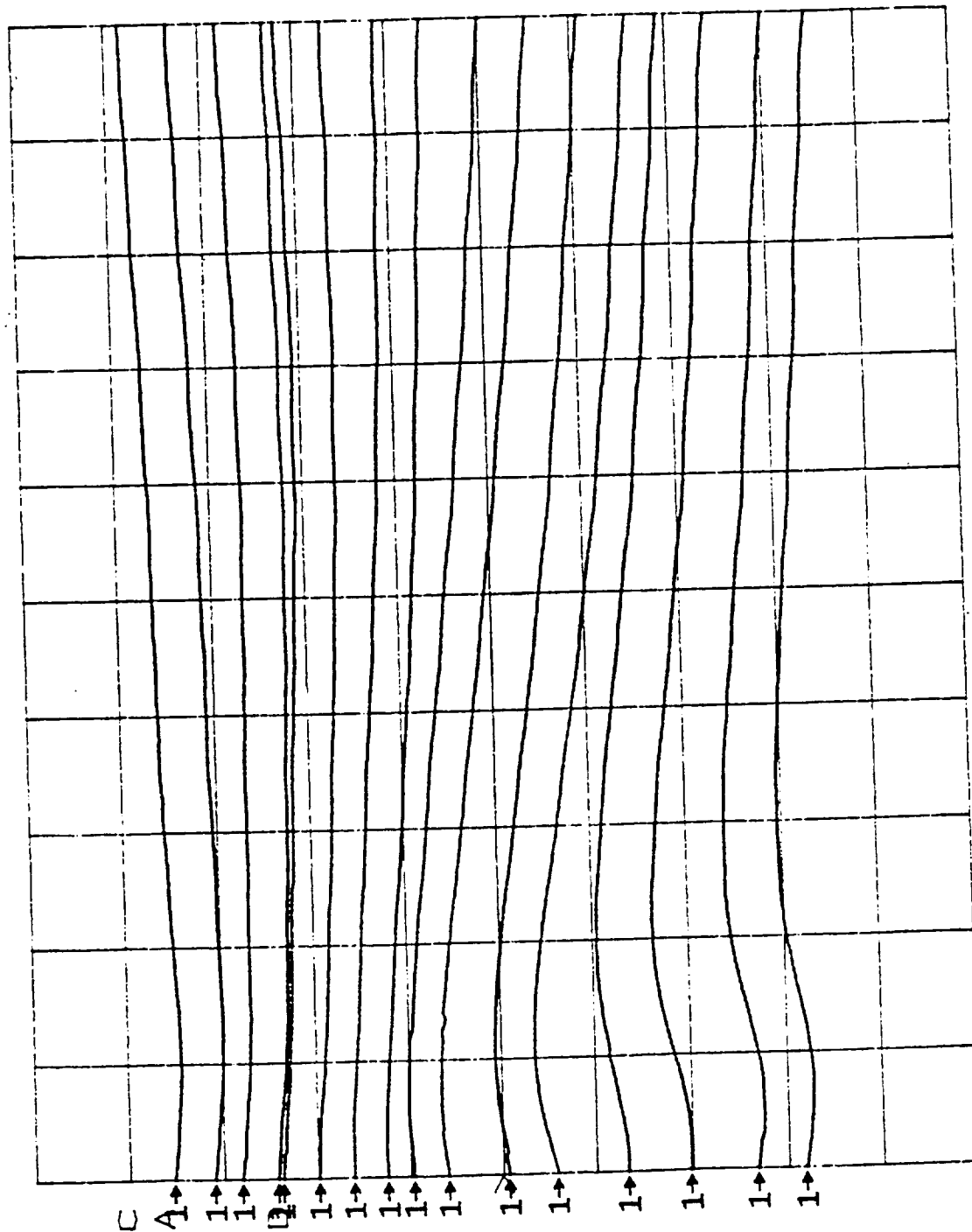
The mask errors were corrected and new plates were made. The recess etching problem was solved by modifying processing of the gate level resist. It was discovered that the poor logic FET characteristics were caused by a thin layer of silicon nitride between the gate and the GaAs. The layer remained after etching the anneal cap due to a difference in etch rate between small open areas and large open areas. The problem was solved by extending the etch time for complete removal of the cap in all areas.

With these problems solved, working phase shifters with on-chip logic were fabricated and demonstrated. The new phase shifter design had two significant features that differed from older designs.

- o The phase shifter chip size was reduced from $2.5 \times 5.5 \times 0.15 \text{ mm}^3$ to $3.2 \times 2.7 \times 0.15 \text{ mm}^3$ by eliminating the reference line on the 180 degree fit and reducing the spacing between lines.
- o On-chip implanted resistors were used to improve the RF decoupling of the switch FETs from the gate bias supply.

RF performance of the phase shifter was evaluated first in the NASA band. The phase shifter was cycled through 16 phase states as shown in Figure 52.

S12 \angle
 REF 0.0 °
 45.0 °/



45 degrees
 Per Division

27.5 GHz START 27.500001600 GHz 30 GHz
 STOP 30.000000000 GHz

Figure 52. Phase Shift for 16 Phase States In NASA Band
 (27.5 - 30 GHz)

Measurement of the insertion loss in the band (Figure 53) showed minimum insertion loss variation with phase near the high end of the band. At the high end of the band the insertion loss was approximately 12.5 dB with a 1 dB insertion loss envelope. Although we have produced phase shifters with lower insertion loss, the insertion loss variation with phase is the lowest we have seen so far. The insertion loss can probably be reduced by lowering the FET on resistance using different switching FET implants. Wafers are presently in process which use implants which we believe will give improved results.

Since the best performance of the phase shifter occurred near the high end of NASA band, we also tested the phase shifter over a band centered at higher frequency where best overall operation was observed. Figures 54 and 55 show the phase shift and insertion loss envelope for the phase shifter over the optimum operating band of 29 to 32.5 GHz. At the present time we do not plan any design changes to lower the optimum operating frequency range since the frequency may change when the FET implants are optimized.

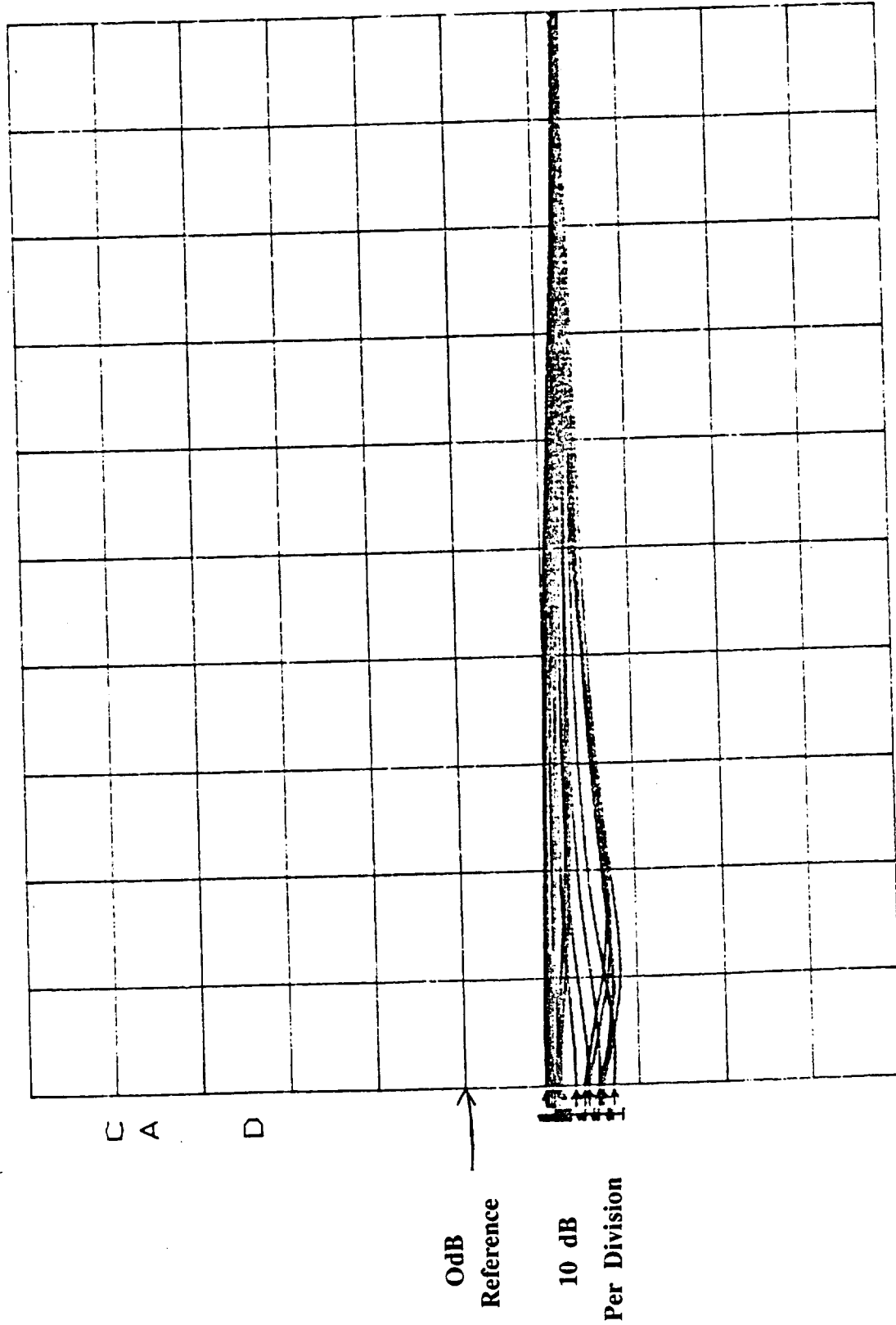
The new phase shifter design also included 2 on-chip logic circuits with two different designs. A photomicrograph of the completed logic circuits is shown in Figure 56. The high speed version functioned and data was taken on the logic transfer characteristics. Figure 57 shows the transfer characteristics of the logic circuit for 3 different drain voltages (4,5, and 6 volts). The logic switches states with an input of between 1.5 and 2 volts.

To check operation of the phase shifter with logic control, the 180 degree bit of the phase shifter was connected so it was switched with on-chip logic. The reasons for doing this were to:

- 1) Demonstrate operations of the on-chip control logic by actually switching a phase bit.
- 2) Identify any problems that might arise through use of on-chip logic.

Although we did not foresee any problems related to use of on-chip logic, we could foresee the possibility that some effect such as backgating could change the behavior of the phase shifter circuit. In operating the phase shifter with on-chip logic, the transmission lines in the phase shifter are floating

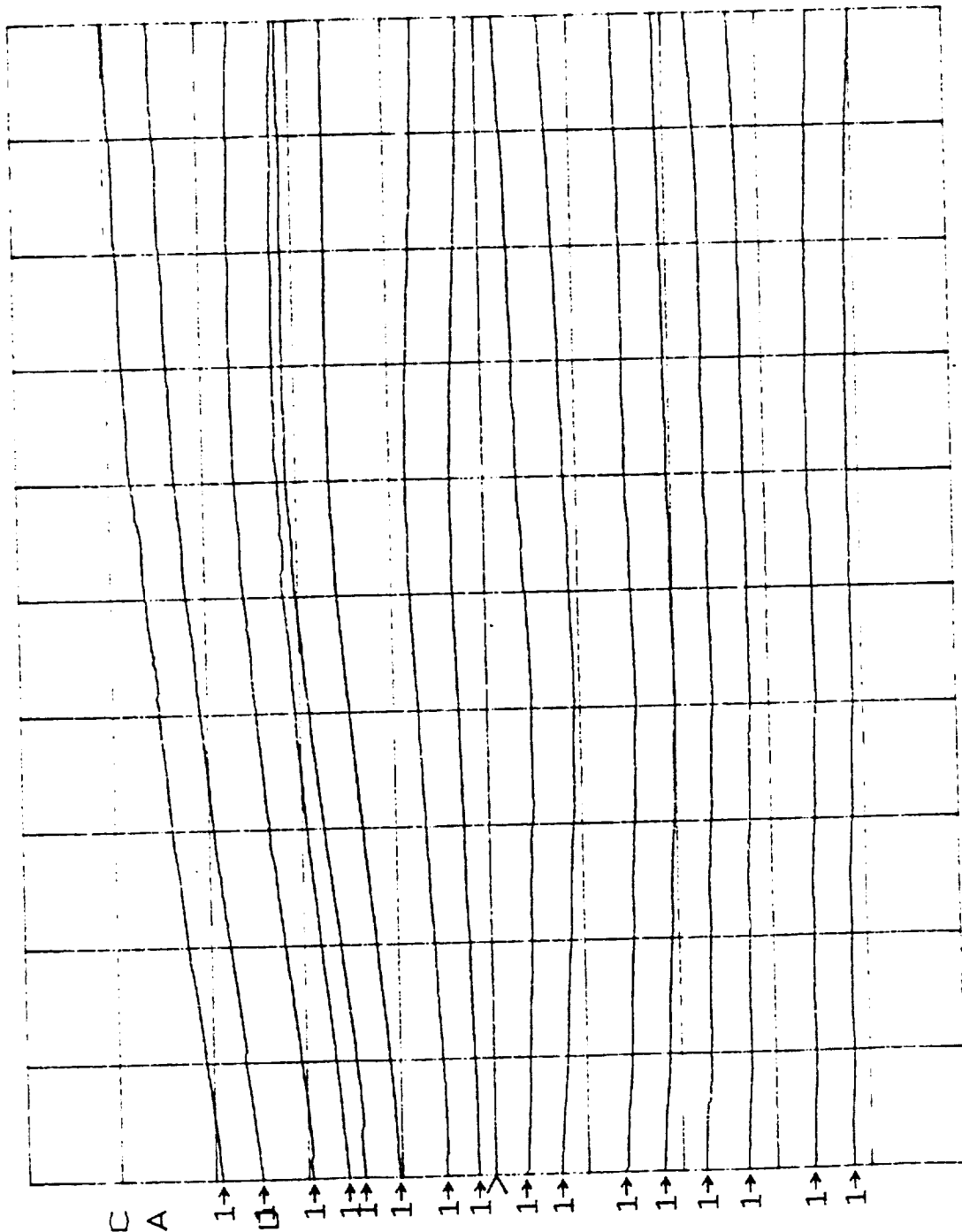
S12 log MAG
 REF 0.0 dB
 10.0 dB/



27.5 GHz START 27.500001600 GHz 30 GHz
 STOP 30.000000000 GHz

Figure 53. Insertion Loss Envelope for 16 Phase States
 in NASA Band

S21 \angle
 REF 0.0 °
 45.0 °/



84 45 Degrees
 Per Division

29 GHz

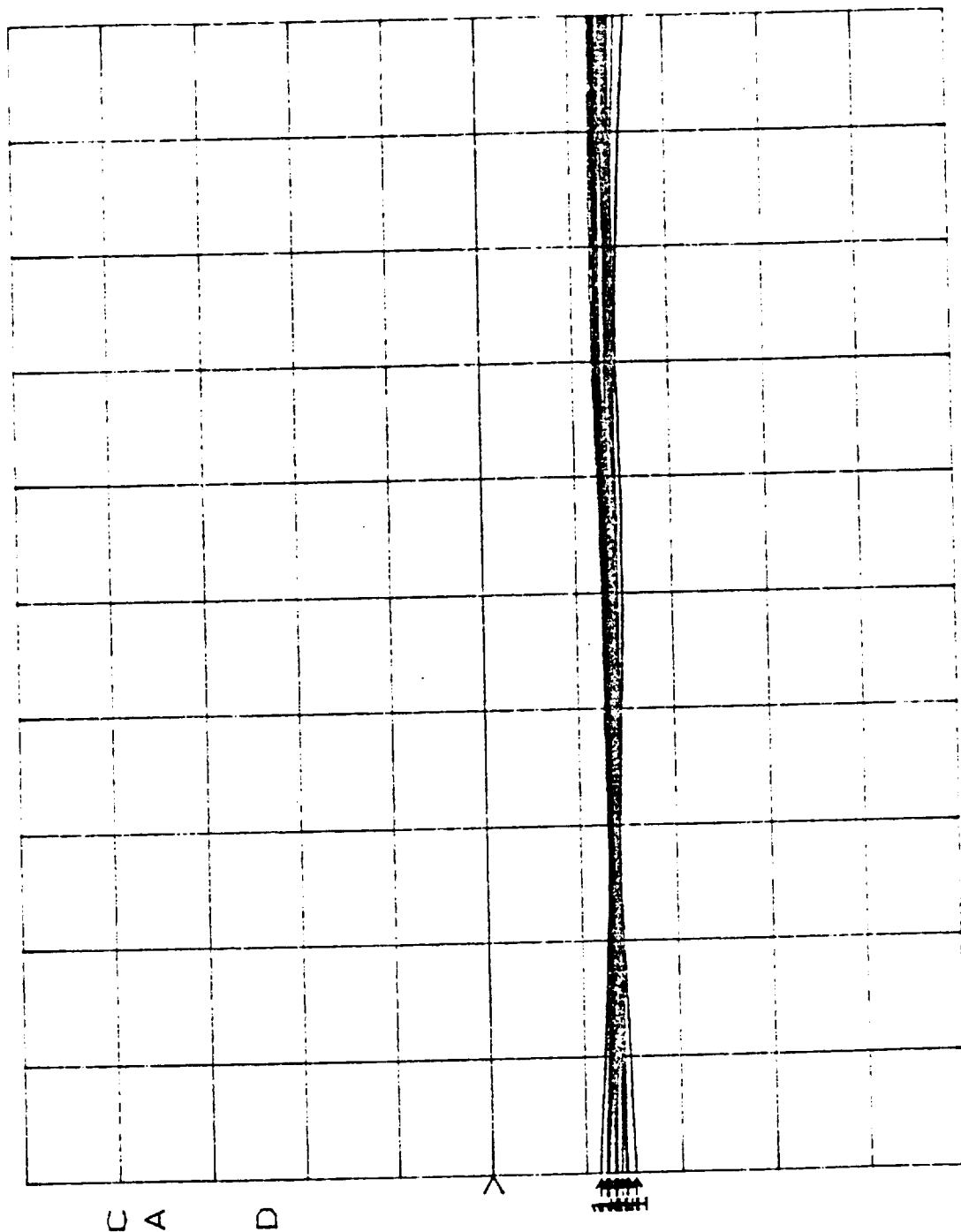
32.5 GHz

START 28.999998408 GHz
 STOP 32.500000008 GHz

Figure 54, Phase Shift for 16 Phase States Over Best

Frequency Range

S21 log MAG
 REF 0.0 dB
 10.0 dB/



32.5 GHz

START 28.999998408 GHz
 STOP 32.500000008 GHz

29 GHz

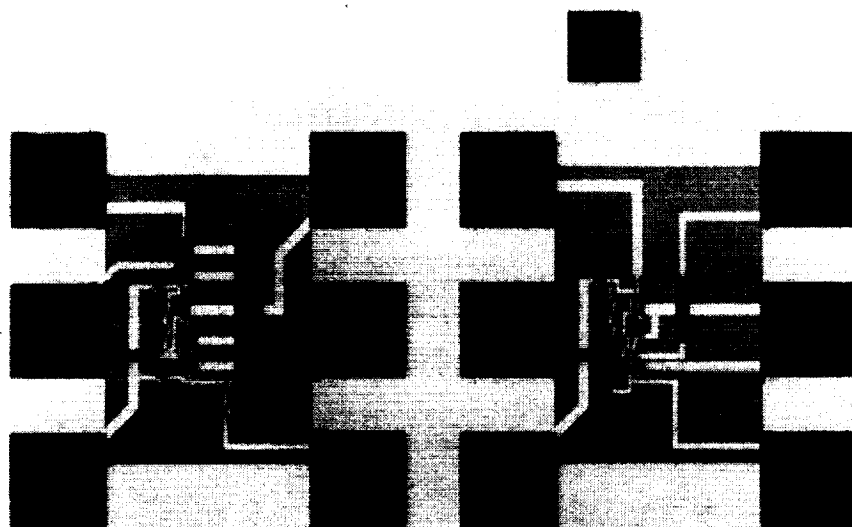
0dB

Reference

10 dB

Per Division

Figure 55. Insertion Loss Envelope for 16 Phase States

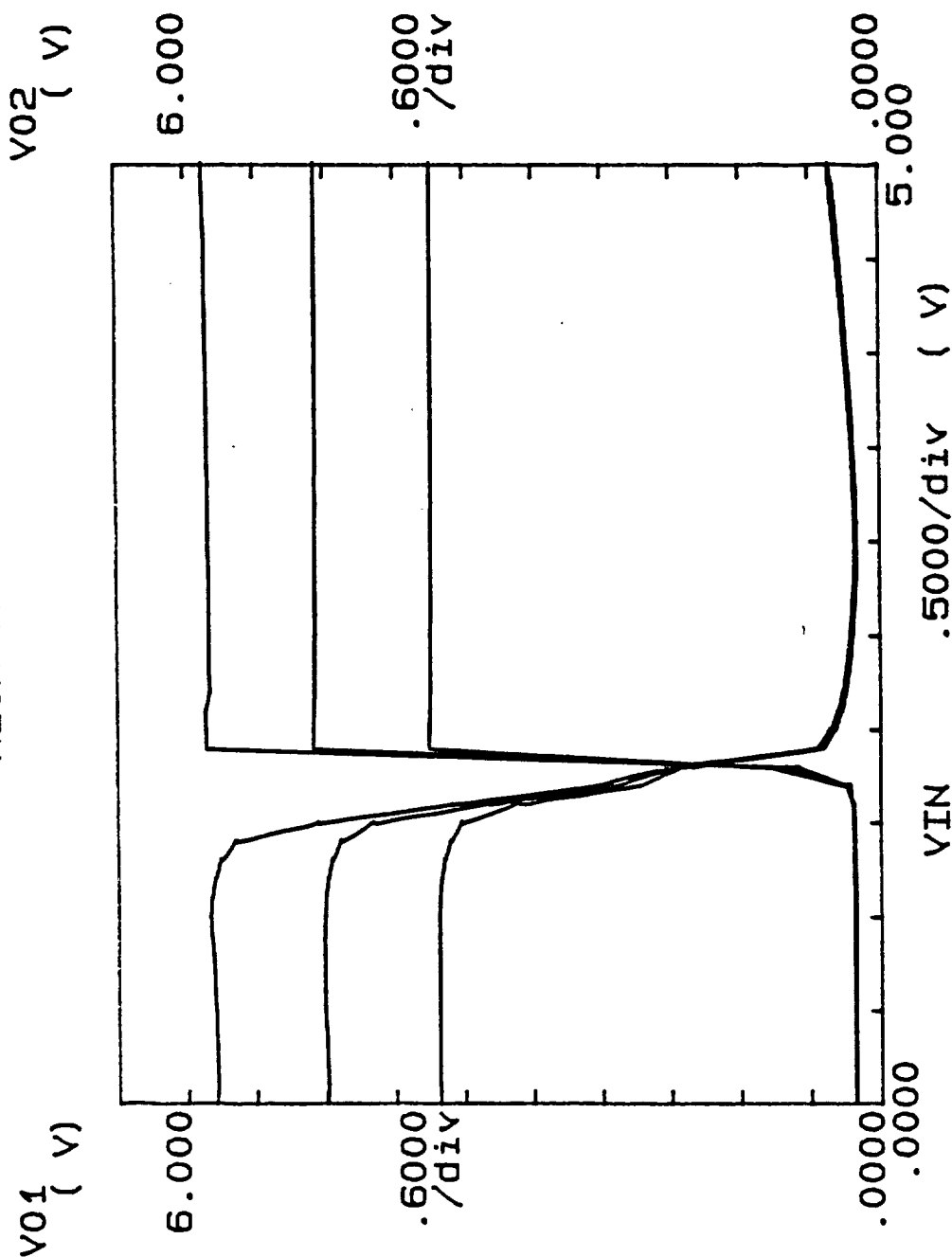


HIGH-SPEED
VERSION

LOW-POWER
VERSION

FIGURE 56. PHOTOMICROGRAPH OF COMPLETED LOGIC CIRCUITS.

***** GRAPHICS PLOT *****
HIGH SPEED P.S. LOGIC



Variable1:
VIN -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

Variable2:
VDD -Ch3
Start 4.0000V
Stop 6.0000V
Step 1.0000V

Constants:
VGN -Ch1 .0000V
VSS -Ch4 -2.5000V

FIGURE 57. TRANSFER CHARACTERISTICS OF ON-CHIP LOGIC USED TO SWITCH 180 DEGREE BIT.

at approximately six volts. The transmission lines must be floated at 6 volts to allow use of TTL input signals to the logic circuits. The logic circuit was connected to the 180 degree bit with bond wires. The phase and insertion loss characteristics for the phase shifter with the 180 degree bit switched by on chip logic are shown in Figure 58 and 59.

The characteristics are similar to those measured earlier with the following exceptions:

- o The phase shifter insertion loss is slightly higher
- o The insertion loss envelope is broader, especially at the lower end of the frequency range.

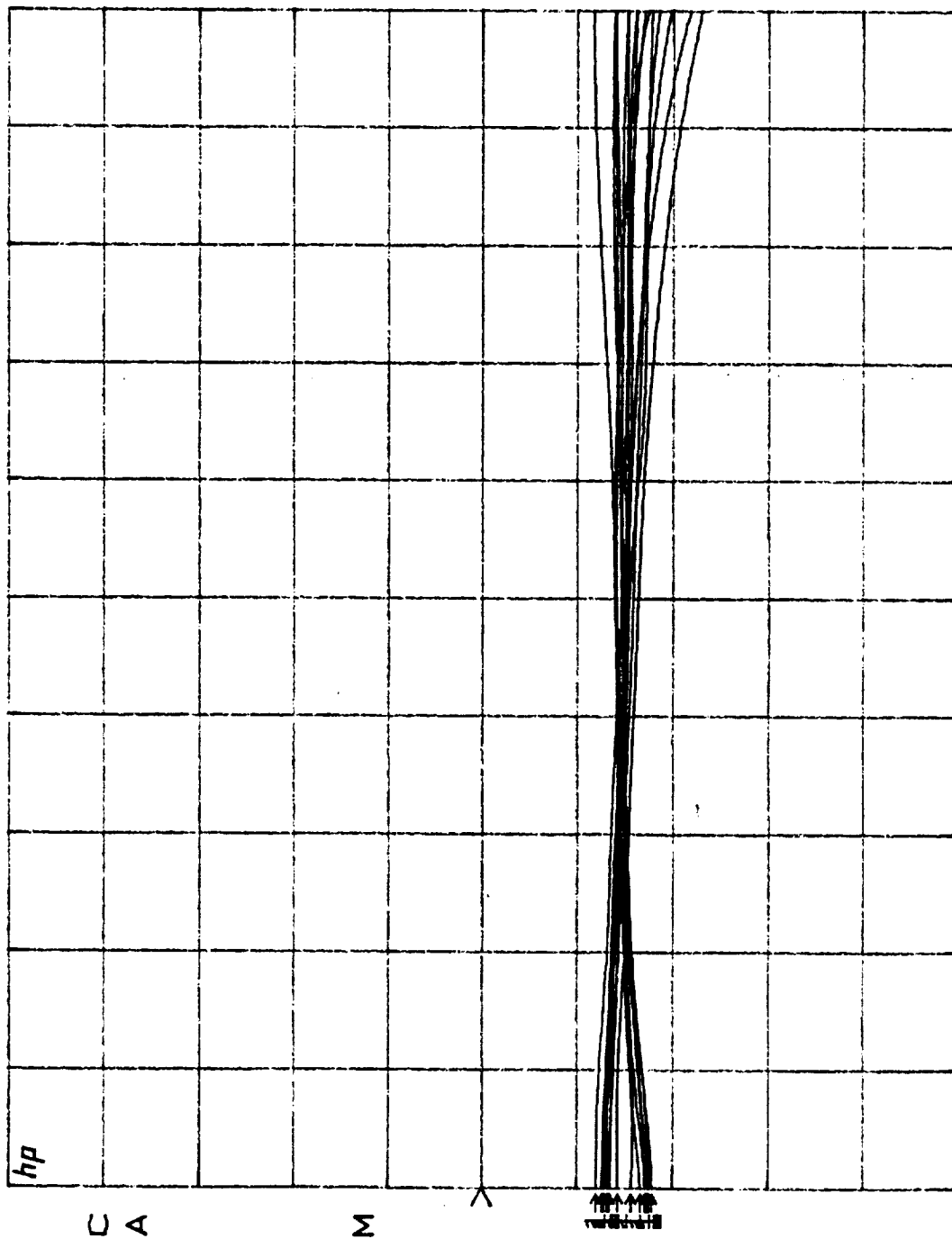
The higher insertion loss can be attributed to the addition of DC blocks required to float the phase shifter transmission lines at 6 volts. The broader insertion loss envelope may be related to the dc blocks or to decoupling of the contact lines. In any event, there is no reason to suspect the influence of on-chip logic since the behavior of the 180 degree bit is similar to all other bits.

3.4 Status and Plans

For the CTS receiver of Task VII, a preliminary integrated circuit incorporating the two-stage LNA, a reduced size phase shifter, and digital control logic has been designed and masks fabricated. During 1987 the fabrication details were worked out to allow all three types of devices to be fabricated on the same chip using selective ion implantation. Initial results were obtained on the reduced size phase shifter and on-chip logic. Results are expected on the two stage LNAs in early 1988.

On the same mask set, along with the LNA/phase shifter/logic circuit, are also included the four and six stage amplifiers. These will be fabricated concurrently with the former ICs and will be tested in 1988 as separate LNA's to be incorporated in up-dated versions of the interconnected receivers. With the high gain (at least 30 dB) six-stage LNA we expect the interconnected receiver noise figure to achieve the original 5 dB goal.

S21 log MAG
 REF 0.0 dB
 10.0 dB/



START 30.00000000 GHz
 STOP 35.00000000 GHz

FIGURE 59. INSERTION LOSS ENVELOPE WITH 180 DEGREE BIT SWITCHED BY ON-CHIP LOGIC.

3.4 Status and Plans

For the CTS receiver of Task VII, a preliminary integrated circuit incorporating the two-stage LNA, a reduced size phase shifter, and digital control logic has been designed and masks fabricated. During 1987 the fabrication details were worked out to allow all three types of devices to be fabricated on the same chip using selective ion implantation. Initial results were obtained on the reduced size phase shifter and on-chip logic. Results are expected on the two stage LNAs in early 1988.

On the same mask set, along with the LNA/phase shifter/logic circuit, are also included the four and six stage amplifiers. These will be fabricated concurrently with the former ICs and will be tested in 1988 as separate LNA's to be incorporated in up-dated versions of the interconnected receivers. With the high gain (at least 30 dB) six-stage LNA we expect the interconnected receiver noise figure to achieve the original 5 dB goal.

Following evaluation of the CTS preliminary circuits, a second design iteration will include the gain control amplifier as well as the LNA and phase shifter. This receiver submodule will be evaluated with the RF/IF submodule (delivered in 1987) to assess the performance of the CTS receiver. A final fabrication pass of the receiver submodule is planned in 1988. Delivery of CTS receivers is planned in 1989.

4.0 PRODUCT ASSURANCE, TECHNOLOGY ASSESSMENT AND REPORTING - TASKS VIII, IX AND X

A product assurance program has been implemented in accordance with the requirements of Section 3.4 of the RFP. Log books concerning device and circuit development and fabrication have been utilized from the outset of the program.

Technology assessment is an on-going activity and includes reporting of results obtained on this contract as well as a comparison of these results relative to that reported by others in the technical literature. A draft copy of the technology assessment report summarizing the state-of-the-art for the

key technology items (30 GHz devices and circuits) in this program has been submitted to NASA.

Reports have included updated work plans, monthly and annual technical progress reports, as well as monthly and quarterly financial and management reports (533M, 533Q, 533P) as required under the contract.

References

1. "Ka-Band Monolithic Gain Control Amplifier", J. Geddes, V. Sokolov, and T. Contolatis, Electronics Letters, Vol.22, No. 9, pp 503-504, April 24, 1986.
2. "Two-Stage Dual Gate MESFET Monolithic Gain Control Amplifier for Ka-Band", V. Sokolov, J. Geddes, and T. Contolatis, to be presented at 1987 IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest pp 75-79.
3. GE Final Report: Vol I, Configuration Study for a 30GHz Monolithic Receive Array, prepared for NASA Lewis Research Center, Cleveland, Ohio, by GE Electronics Laboratory, Syracuse, NY under Contract NAS3-23780, Nov. 1, 1984.
4. "Characteristics of 30 GHz MMIC Receiver for Satellite Feed Array Applications", J. Geddes, V. Sokolov, D. Carlson, P. Bauhahn, and R. Romanofsky, 1987 GaAs IC Symposium Technical Digest, pp 155-158.

APPENDIX A

SUBMODULE DATA

LNA bias conditions for figures A-1 thru A-3

STAGE 1: $V_{GS} = -0.55 \text{ V}$
 $V_{DS} = 2.41 \text{ V}$
 $I_{DS} = 36.3 \text{ mA}$

STAGE 2: $V_{GS} = -2.72 \text{ V}$
 $V_{DS} = 1.9 \text{ V}$
 $I_{DS} = 7.4 \text{ mA}$

LNA bias conditions for figures A-4 thru A-6

STAGE 1: $V_{GS} = -2.56 \text{ V}$
 $V_{DS} = 1.21 \text{ V}$
 $I_{DS} = 9.7 \text{ mA}$

STAGE 2: $V_{GS} = -2.72 \text{ V}$
 $V_{DS} = 1.9 \text{ V}$
 $I_{DS} = 7.3 \text{ V}$

Phase shifter bias conditions for figures A-7 thru A-10

Switched line bits: $V_{GS} = -5.5 \text{ V or } 0.0 \text{ V}$

Loaded line bit: $V_{GS} = -5.5 \text{ V (Ref)}$
 or
 $V_{GS} = -2.5 \text{ V (Delay)}$

GCA bias conditions for figures A-11 thru A-14

STAGE 1: $V_{GS} (1) = -0.74 \text{ V}$
 $V_{DS} = 4.0 \text{ V}$

STAGE 2: $V_{GS} (1) = -0.74 \text{ V}$
 $V_{DS} = 4.0 \text{ V}$

GAIN SETTING	STAGE 1 AND 2	STAGE 1	STAGE 2
(dB)	$V_{GS} (2)$ (V)	I_{DS} (mA)	I_{DS} (mA)
18	-0.14	30.1	31.9
15	-0.27	29.6	31.4
12	-0.40	29.0	30.8
9	-0.51	28.4	30.2
6	-0.62	27.7	29.5
3	-0.74	26.9	28.7
0	-0.89	25.7	27.5
-3	-1.09	24.1	25.8
-6	-1.36	21.7	23.4
-9	-1.70	18.7	20.3
-12	-2.08	15.4	17.0
-15	-2.42	12.6	14.1
-18	-2.73	10.1	11.6

GCA Bias Conditions for Figures A-15 thru A-18.

STAGE 1: $V_{GS} (1) = -0.88V$
 $V_{DS} = 2.9V$

STAGE 2: $V_{GS} (1) = -0.76V$
 $V_{DS} = 3.4V$

GAIN SETTING	STAGE 1 AND 2	STAGE 1	STAGE 2
(dB)	$V_{GS} (2)$ (V)	I_{DS} (mA)	I_{DS} (mA)
12	-0.24	28.5	31.3
9	-0.41	27.9	30.6
6	-0.55	27.2	29.8
3	-0.68	26.5	29.0
0	-0.82	25.5	27.9
-3	-0.98	24.2	26.5
-6	-1.21	22.3	24.4
-9	-1.48	19.8	21.9
-12	-1.86	16.3	18.4

GCA Bias Conditions for Figures A-19 thru A-22.

STAGE 1: $V_{GS} (1) = -0.88V$
 $V_{DS} = 2.9V$

STAGE 2: $V_{GS} (1) = -0.76V$
 $V_{DS} = 3.4V$

GAIN SETTING	STAGE 1 AND 2	STAGE 1	STAGE 2
(dB)	$V_{GS} (2)$ (V)	I_{DS} (mA)	I_{DS} (mA)
12	-0.24	28.5	31.3
9	-0.41	27.9	30.6
6	-0.55	27.2	29.8
2	-0.73	26.2	28.6
-1	-0.87	25.2	27.5

FIGURE CAPTIONS FOR APPENDIX A

- Figure A-1 Input Return Loss Versus Frequency for Modified Two-Stage Low Noise Amplifier from Wafer DG-85 at High Gain Bias.
- Figure A-2 Gain Versus Frequency for Modified Two-Stage Low Noise Amplifier from Wafer DG-85 at High Gain Bias.
- Figure A-3 Output Return Loss Versus Frequency for Modified Two-Stage Low Noise Amplifier from Wafer DG-85 at High Gain Bias.
- Figure A-4 Input Return Loss Versus Frequency for Modified Two-Stage Low Noise Amplifier from Wafer DG-85 at Low Noise Bias.
- Figure A-5 Gain Versus Frequency for Modified Two-Stage Low Noise Amplifier from Wafer DG-85 at Low Noise Bias.
- Figure A-6 Output Return Loss Versus Frequency for Modified Two-Stage Low Noise Amplifier from Wafer DG-85 at Low Noise Bias.
- Figure A-7 Input Return Loss Versus Frequency for Phase Shifter from Wafer PS-09 (Superposition of 16 States of Phase Shifter).
- Figure A-8 Insertion Loss Versus Frequency for Phase Shifter from Wafer PS-09 (Superposition of 16 States of Phase Shifter).
- Figure A-9 Insertion Phase Versus Frequency for Phase Shifter from Wafer PS-09 (Superposition of 16 States of Phase Shifter).
- Figure A-10 Output Return Loss Versus Frequency for Phase Shifter from Wafer PS-09 (Superposition of 16 States of Phase Shifter).
- Figure A-11 Input Return Loss Versus Frequency for Unmodified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 13 Gain States of Gain Control Amplifier).

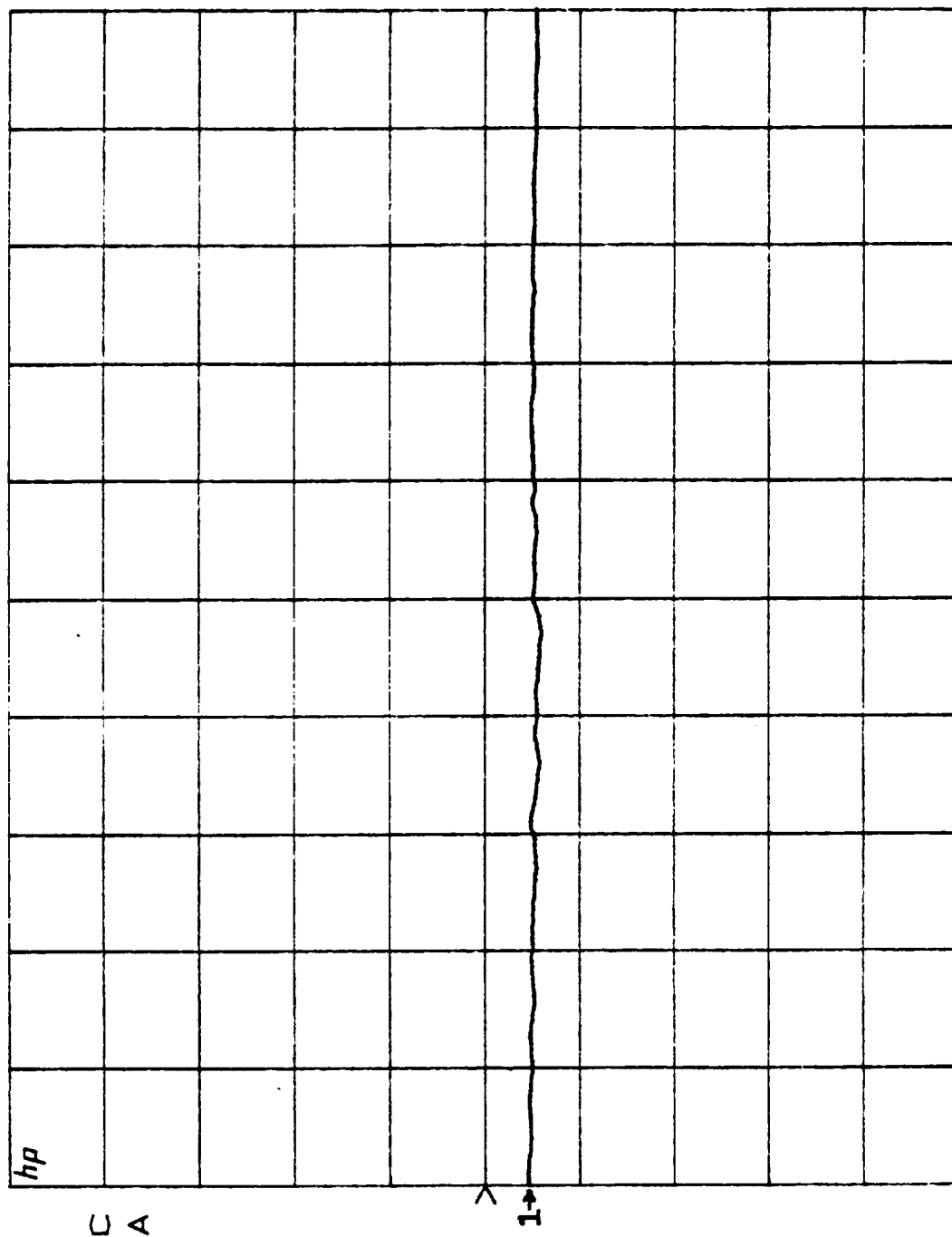
- Figure A-12 Gain Versus Frequency for Unmodified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 13 States of Gain Control Amplifier).
- Figure A-13 Insertion Phase Versus Frequency for Unmodified Two-Stage Gain Control from Wafer DG-85 (Superposition of 13 States of Gain Control Amplifier).
- Figure A-14 Output Return Loss Versus Frequency for Unmodified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 13 States of Gain Control Amplifier).
- Figure A-15 Input Return Loss Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 9 States of Gain Control Amplifier).
- Figure A-16 Gain Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Super Position of 9 States of Gain Control Amplifier).
- Figure A-17 Insertion Phase Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 9 States of Gain Control Amplifier).
- Figure A-18 Output Return Loss Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 9 States of Gain Control Amplifier).
- Figure A-19 Input Return Loss Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 5 States of Gain Control Amplifier).
- Figure A-20 Gain Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 5 States of Gain Control Amplifier).
- Figure A-21 Insertion Phase Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 5 States of Gain Control Amplifier).

Figure A-22 Output Return Loss Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 5 States of Gain Control Amplifier).

Figure A-23 Input Return Loss Versus Frequency for Antipodal Fin-line Transition Used in the First Interconnected Receive Module.

Figure A-24 Insertion Loss Versus Frequency for Antipodal Fin-line Transition Used in the First Interconnected Receive Module.

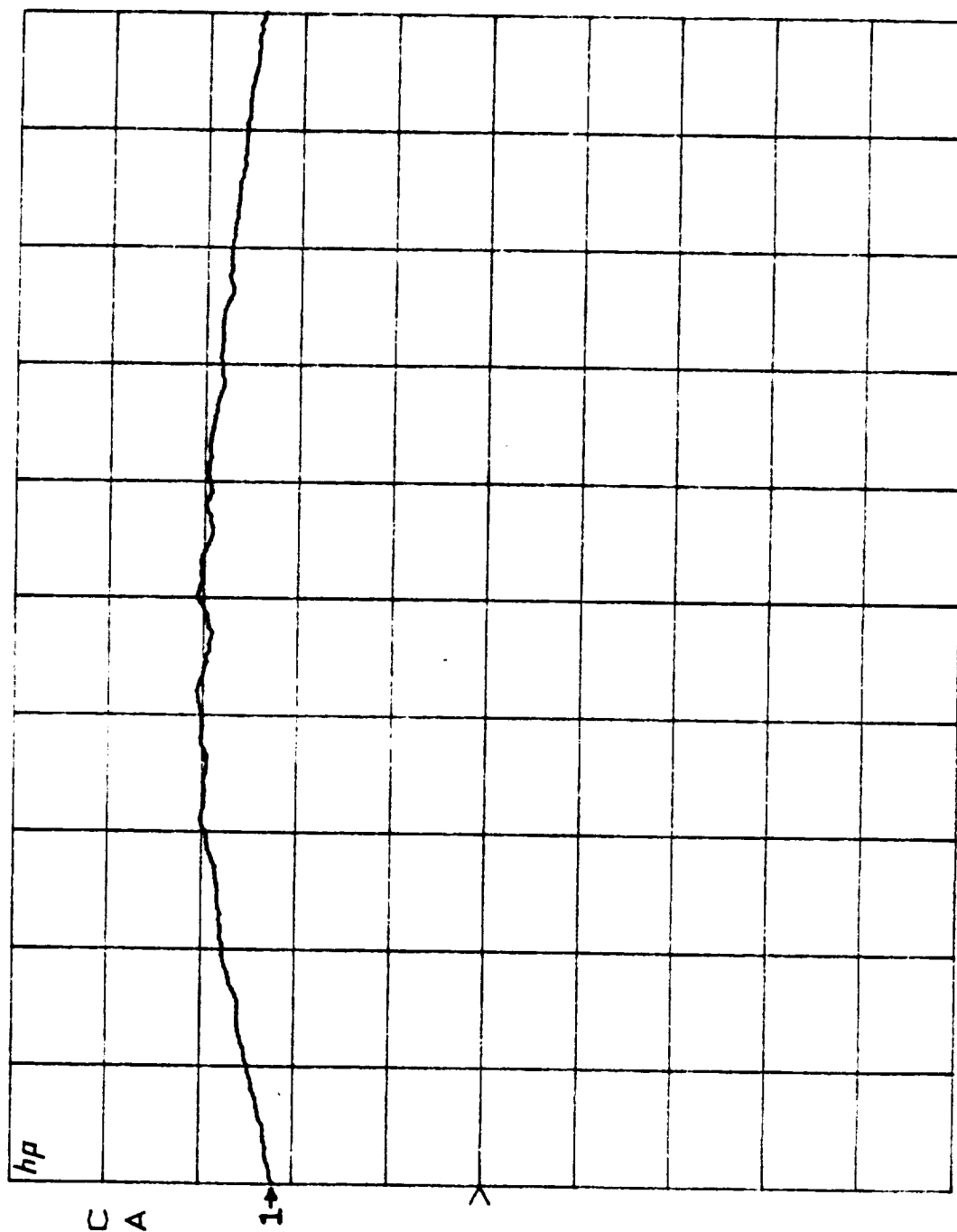
S11 log MAG
 REF 0.0 dB
 10.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-1. Input Return Loss Versus Frequency for Modified Two-Stage Low Noise Amplifier from Wafer DG-85 at High Gain Bias.

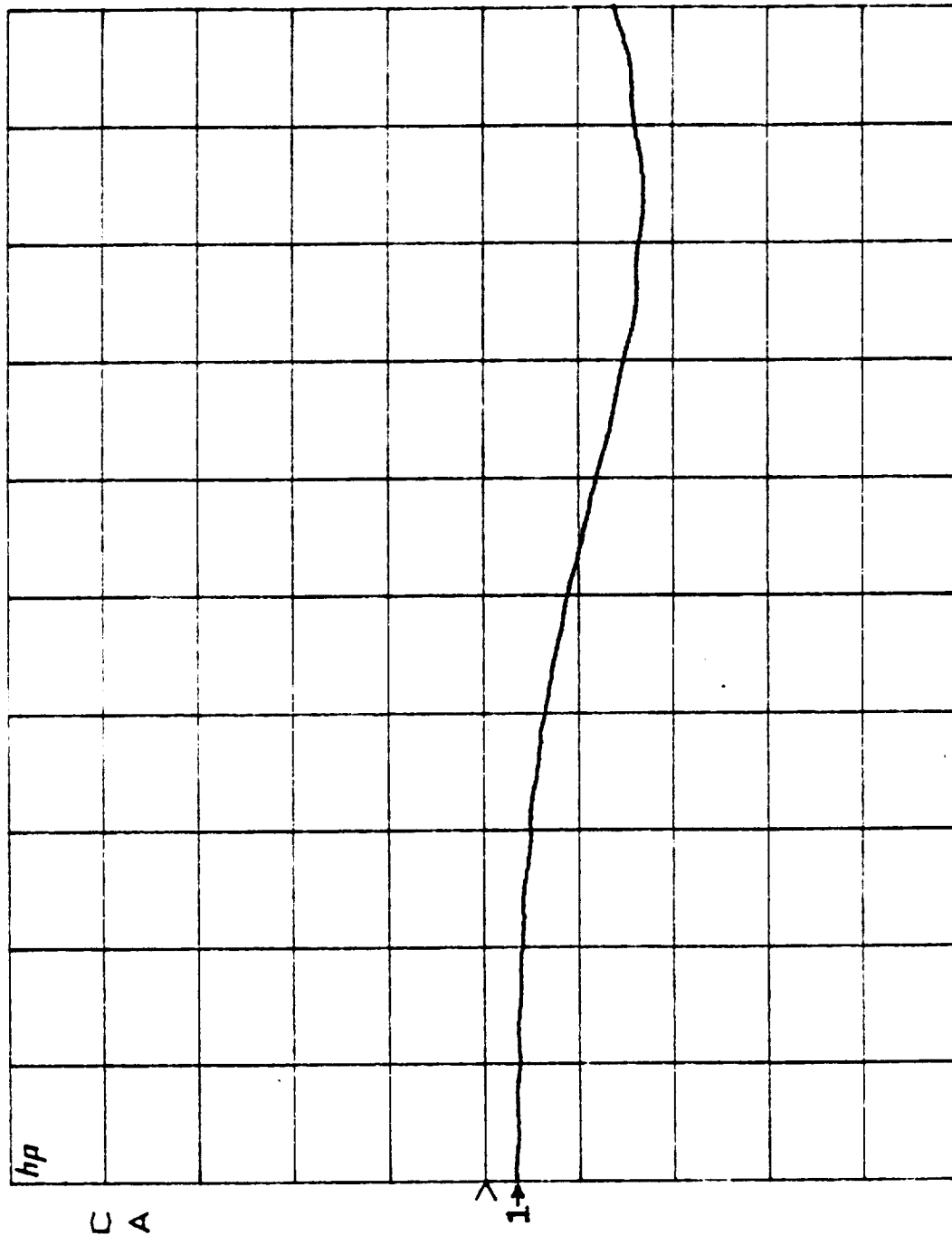
S21 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-2. Gain Versus Frequency for Modified Two-Stage Low Noise Amplifier from Wafer DG-85 at High Gain Bias.

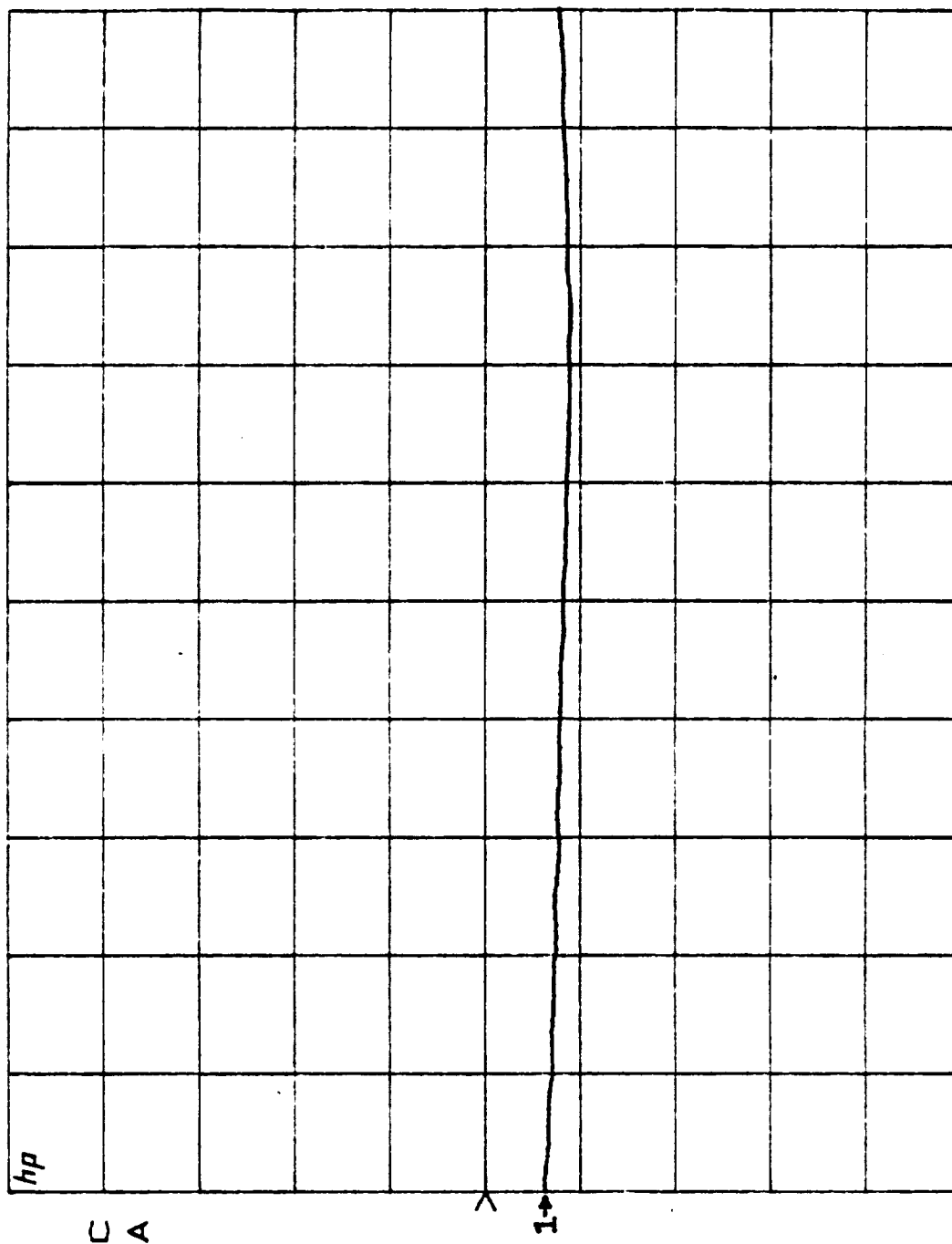
S22 log MAG
 REF 0.0 dB
 10.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-3. Output Return Loss Versus Frequency for Modified Two-Stage Low Noise Amplifier from Wafer DG-85 at High Gain Bias.

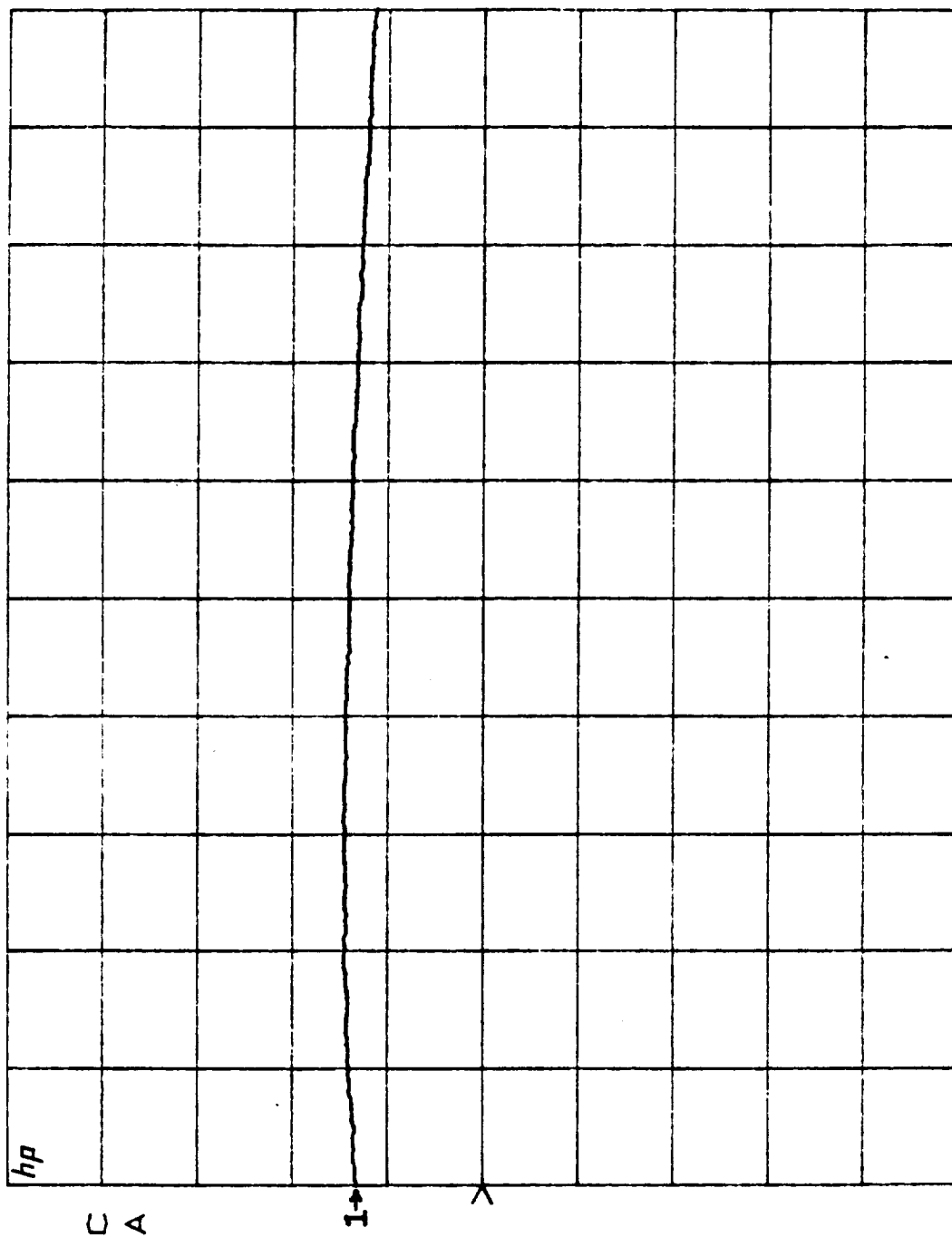
S11 log MAG
 REF 0.0 dB
 10.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-4. Input Return Loss Versus Frequency for Modified Two-Stage Low Noise Amplifier from Wafer DG-85 at Low Noise Bias.

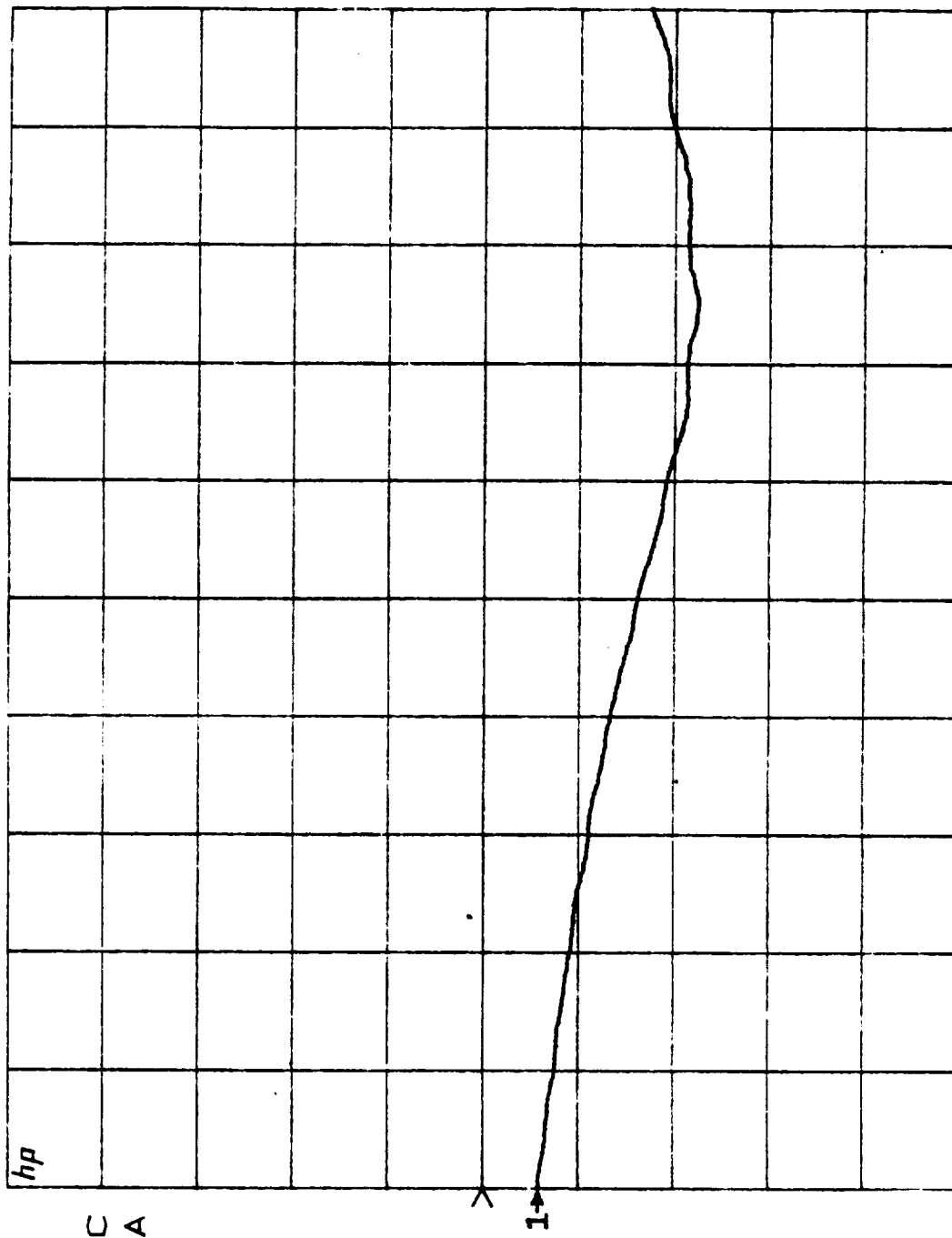
S21 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-5. Gain Versus Frequency for Modified Two-Stage Low Noise Amplifier from Wafer DG-85 at Low Noise Bias.

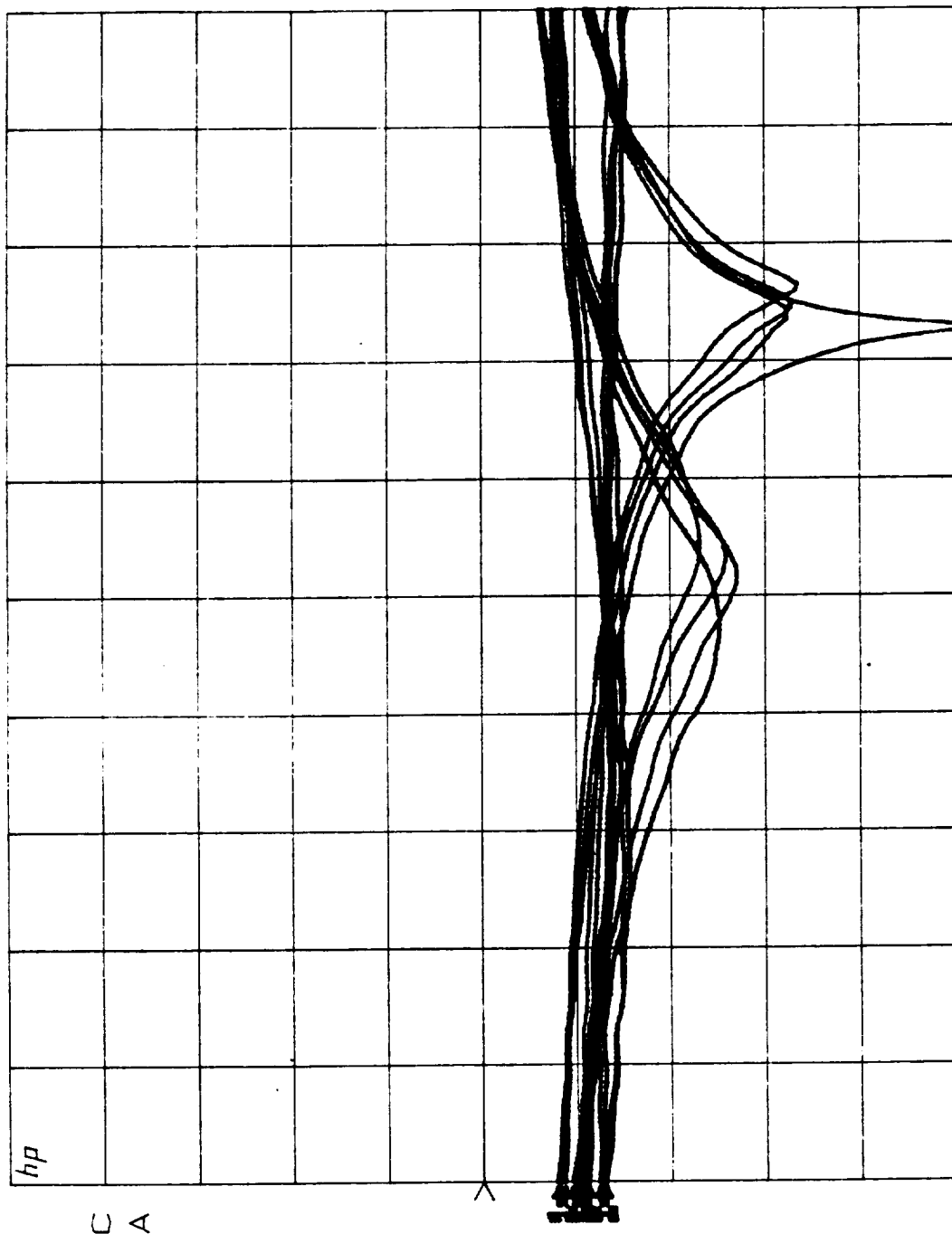
S22 log MAG
 REF 0.0 dB
 10.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-6. Output Return Loss Versus Frequency for Modified Two-Stage Low Noise Amplifier from Wafer DG-85 at Low Noise Bias.

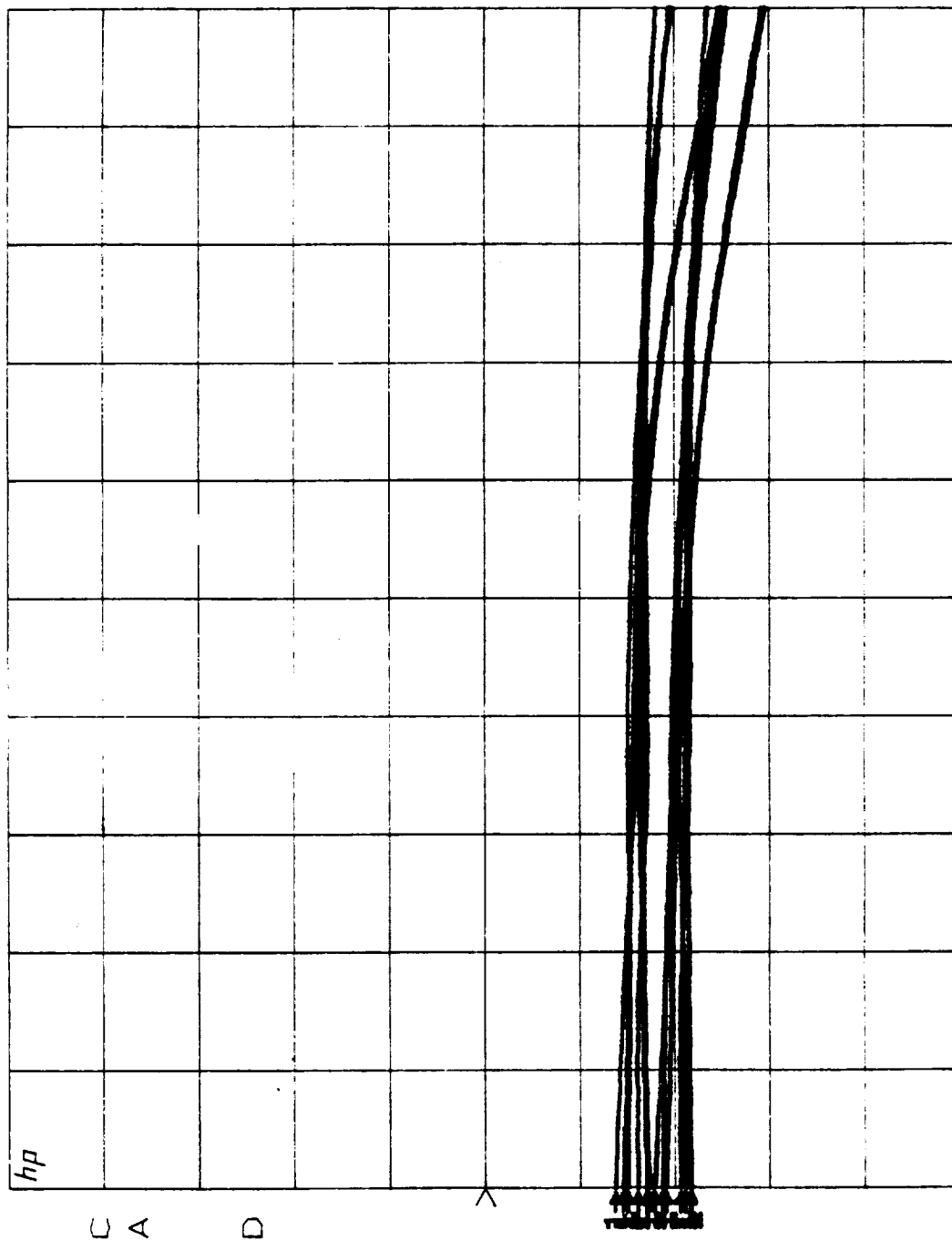
S11 log MAG
 REF 0.0 dB
 10.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-7. Input Return Loss Versus Frequency for Phase Shifter from Wafer PS-09
 (Superposition of 16 States of Phase Shifter).

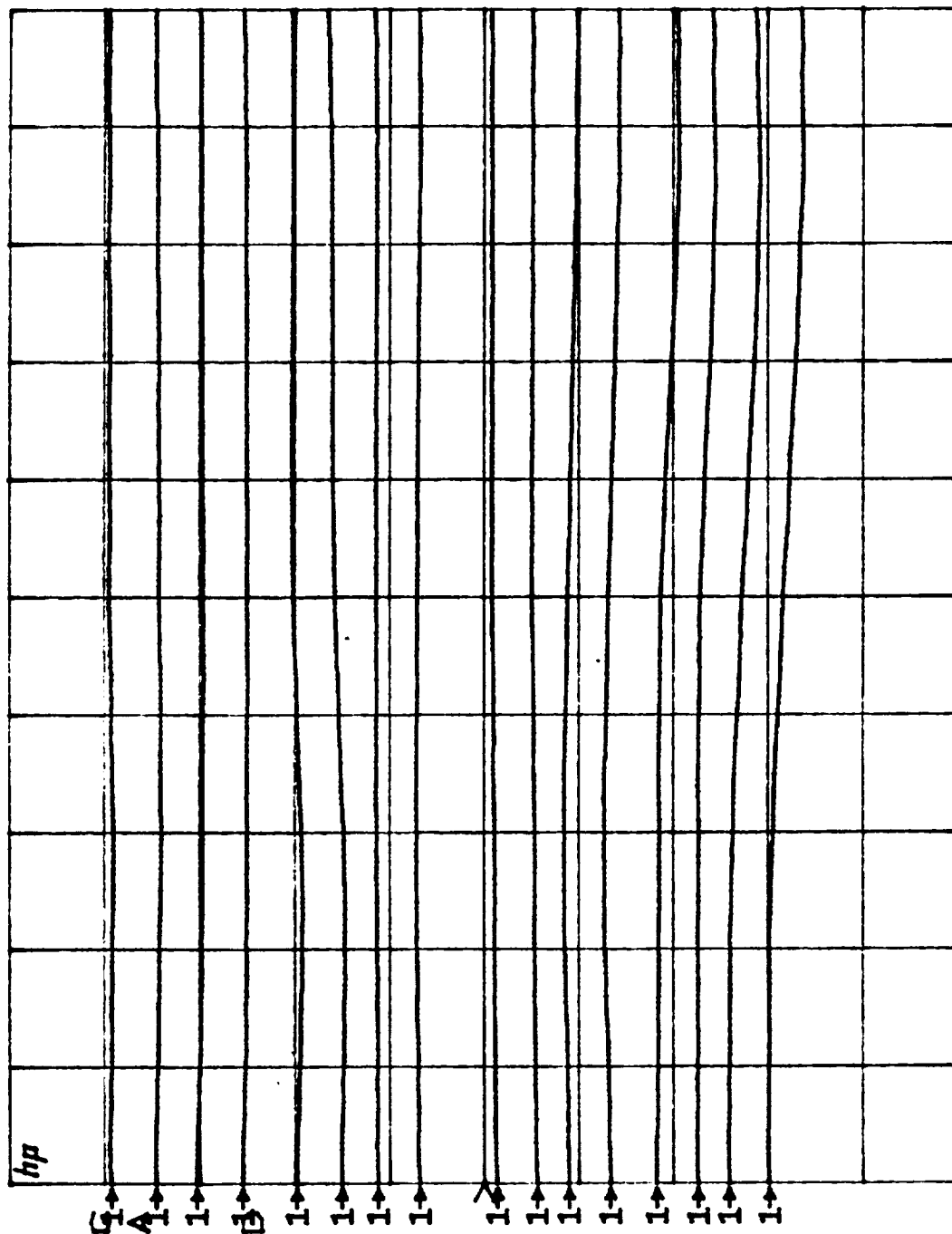
S21 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-8. Insertion Loss Versus Frequency for Phase Shifter from Wafer PS-09 (Superposition of 16 States of Phase Shifter).

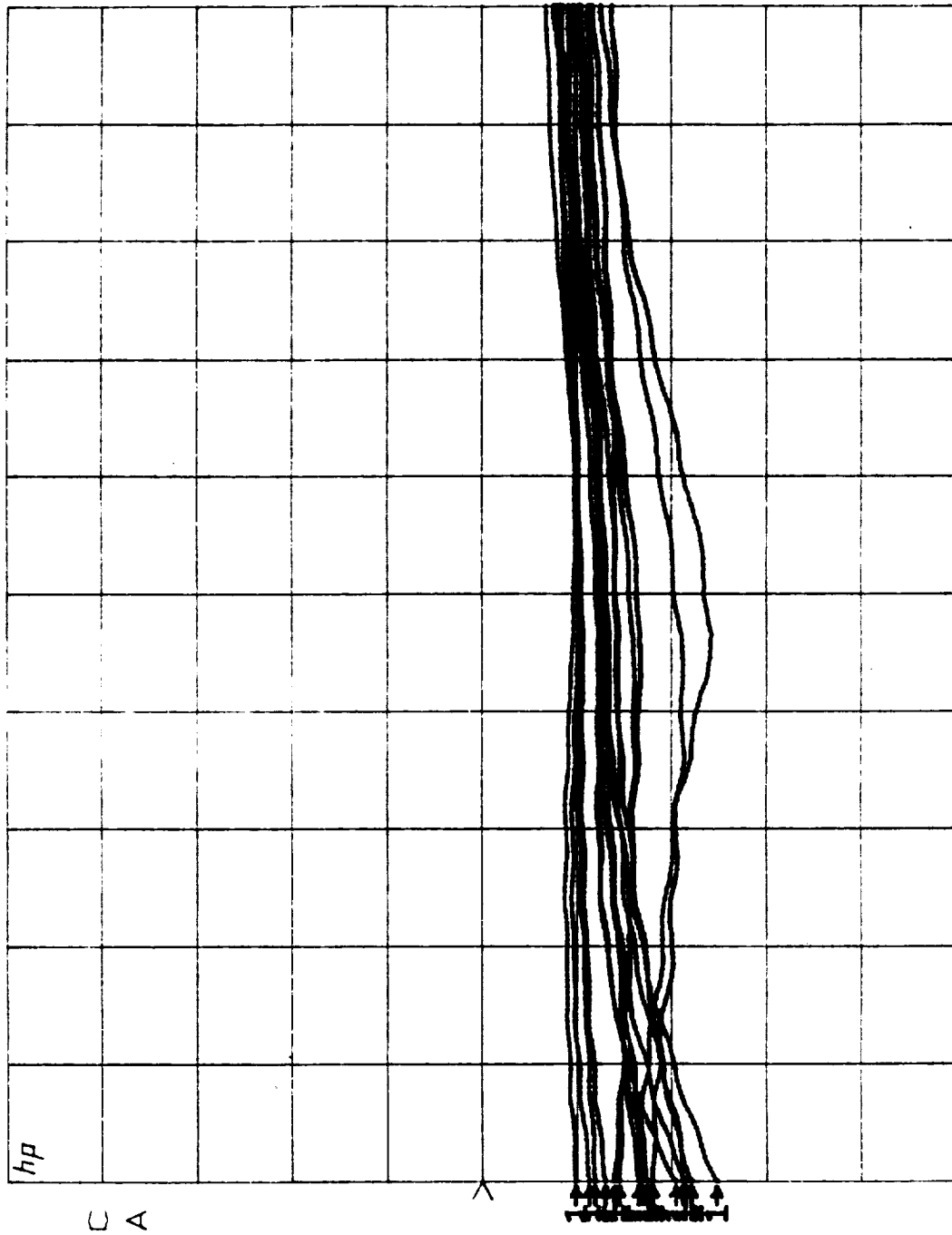
S21 0.0 ° /
 REF 45.0 ° /



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-9. Insertion Phase Versus Frequency for Phase Shifter from Wafer PS-09 (Superposition of 16 States of Phase Shifter).

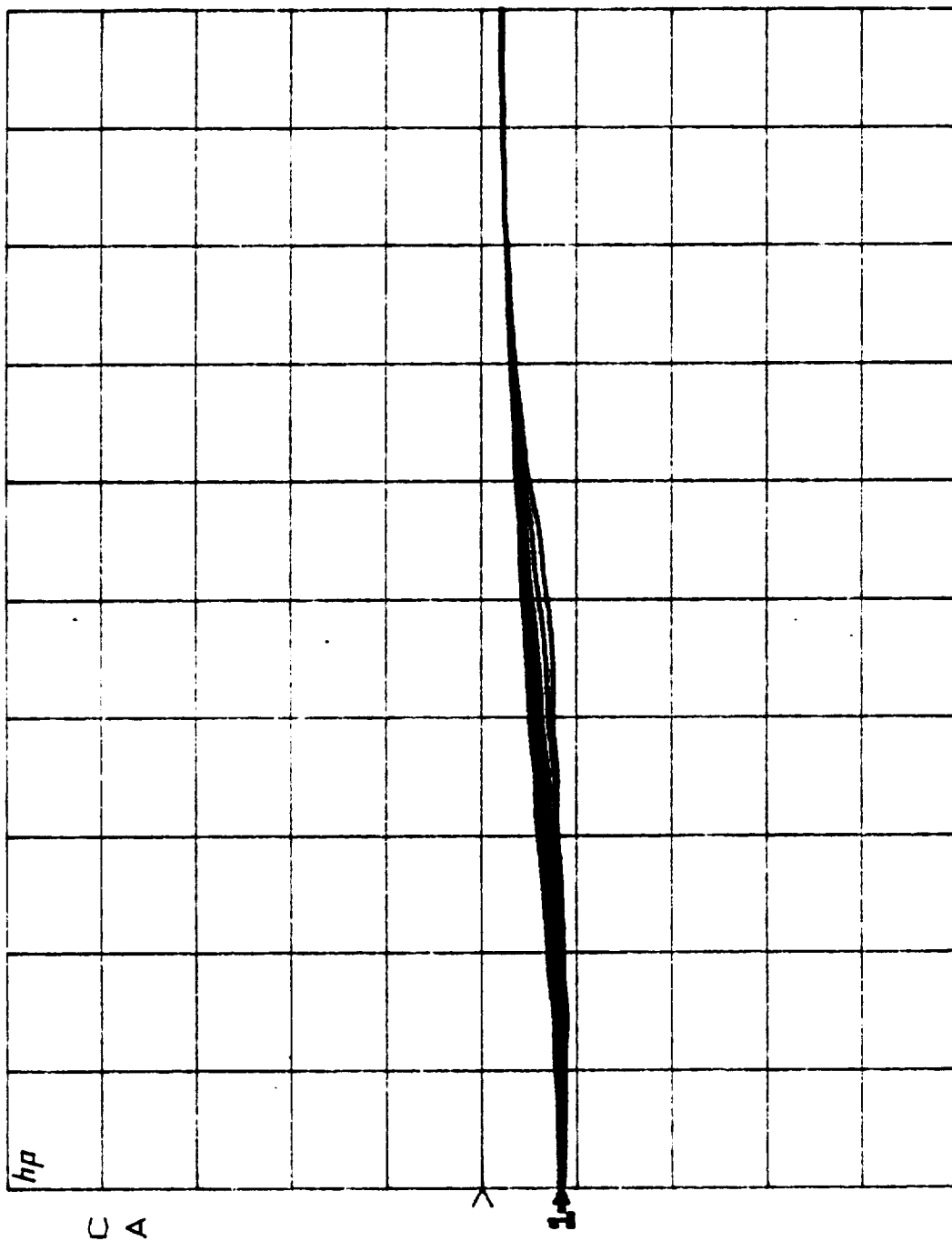
S22 log MAG
 REF 0.0 dB
 10.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-10. Output Return Loss Versus Frequency for Phase Shifter from Wafer PS-09 (Superposition of 16 States of Phase Shifter).

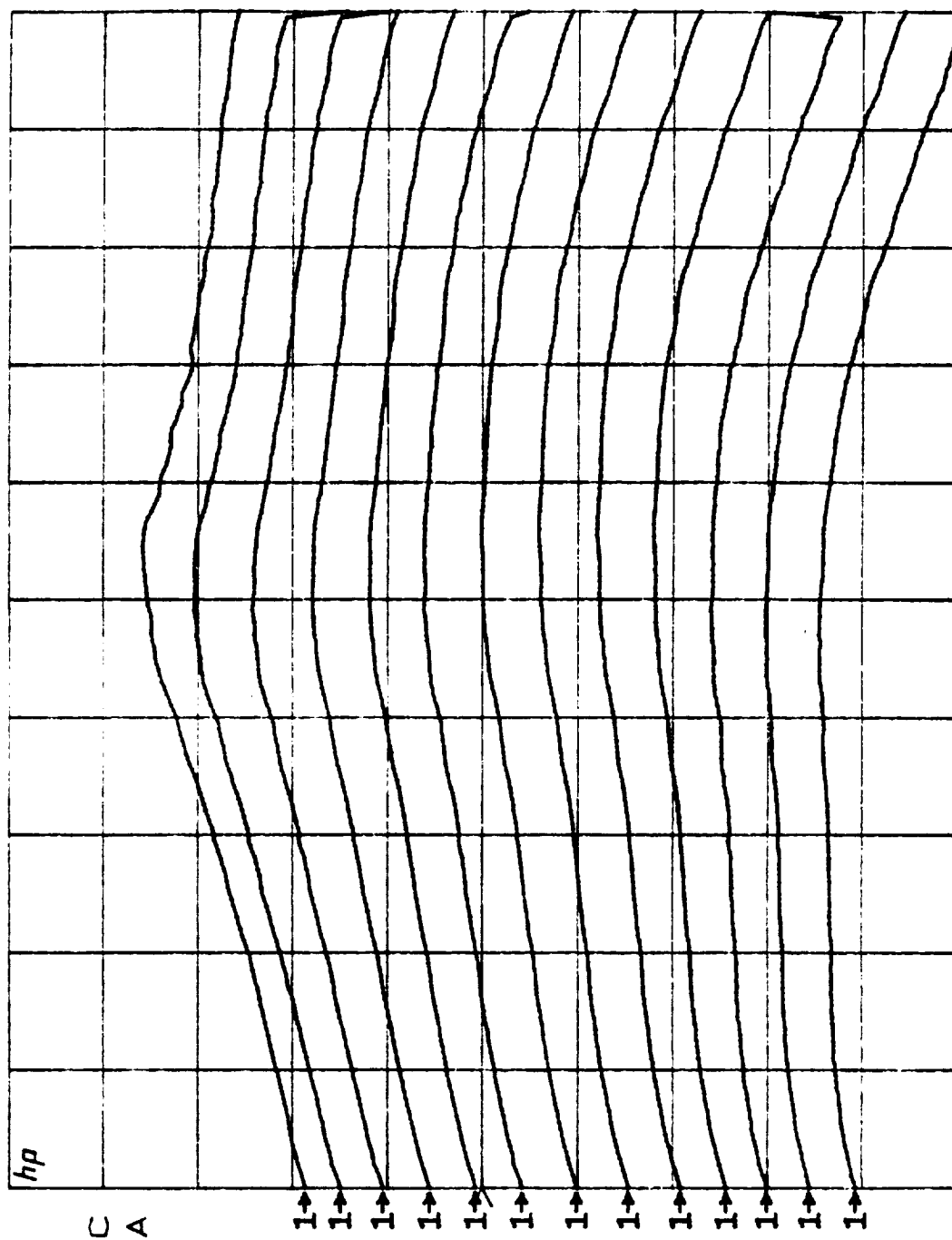
S11 log MAG
 REF 0.0 dB
 10.0 dB/



START 29.000001600 GHz
 STOP 31.500000000 GHz

Figure A-11. Input Return Loss Versus Frequency for Unmodified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 13 Gain States of Gain Control Amplifier).

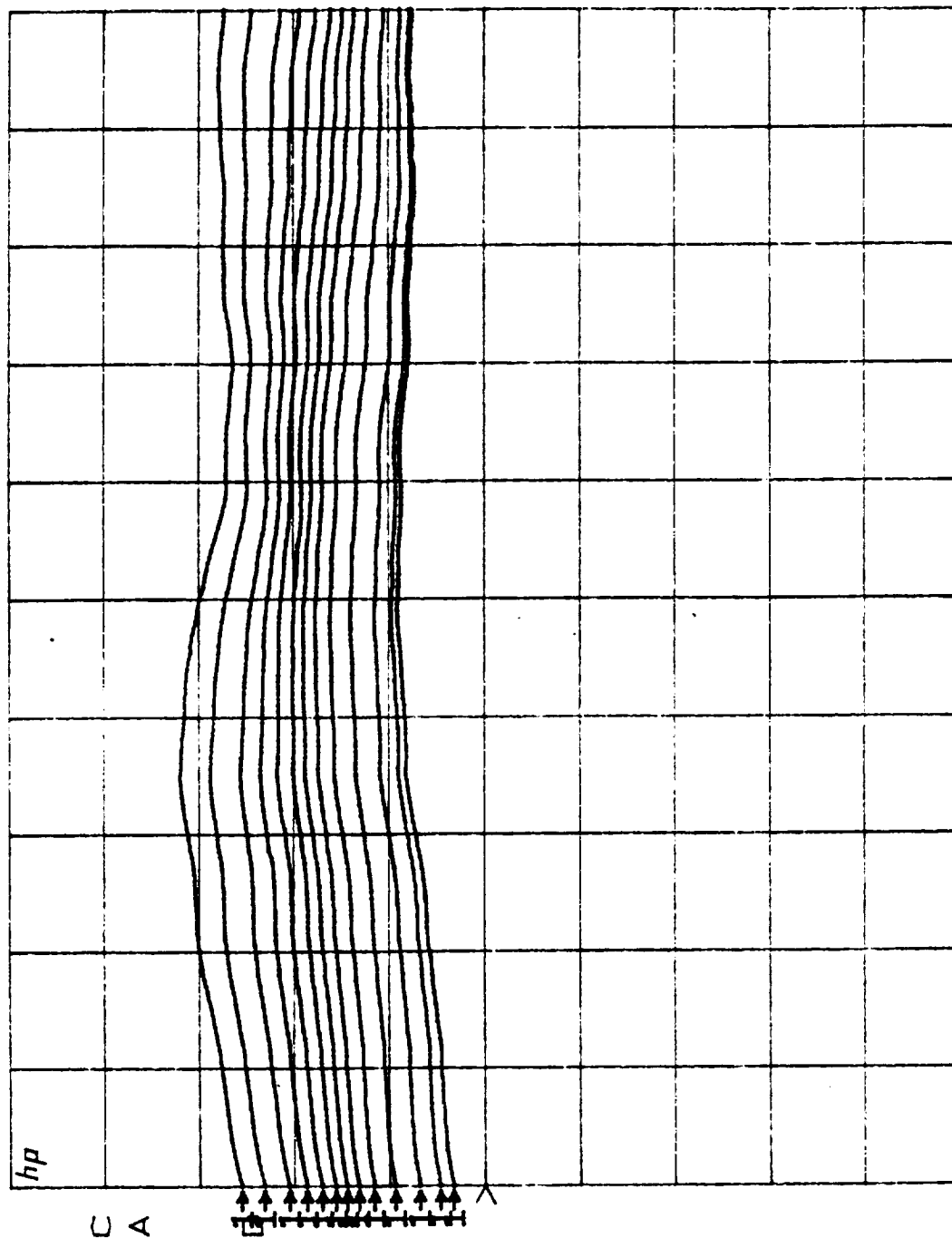
S21 log MAG
 REF 0.0 dB
 5.0 dB/



START 29.000001600 GHz
 STOP 31.500000000 GHz

Figure A-12. Gain Versus Frequency for Unmodified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 13 States of Gain Control Amplifier).

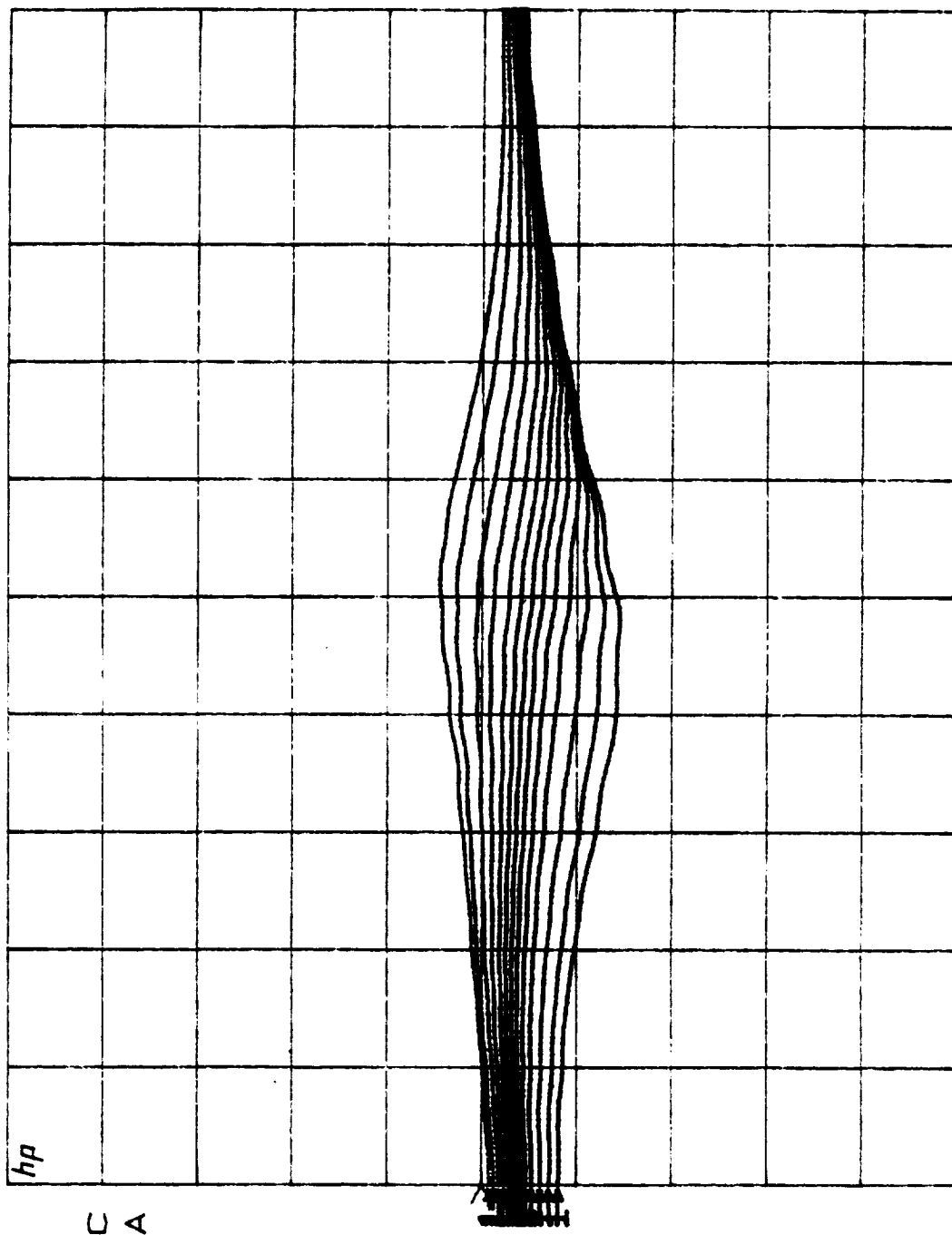
S21 \angle
 REF 0.0 °
 45.0 °/



START 29.000001600, GHz
 STOP 31.500000000 GHz

Figure A-13. Insertion Phase Versus Frequency for Unmodified Two-Stage Gain Control from Wafer DG-85 (Superposition of 13 States of Gain Control Amplifier).

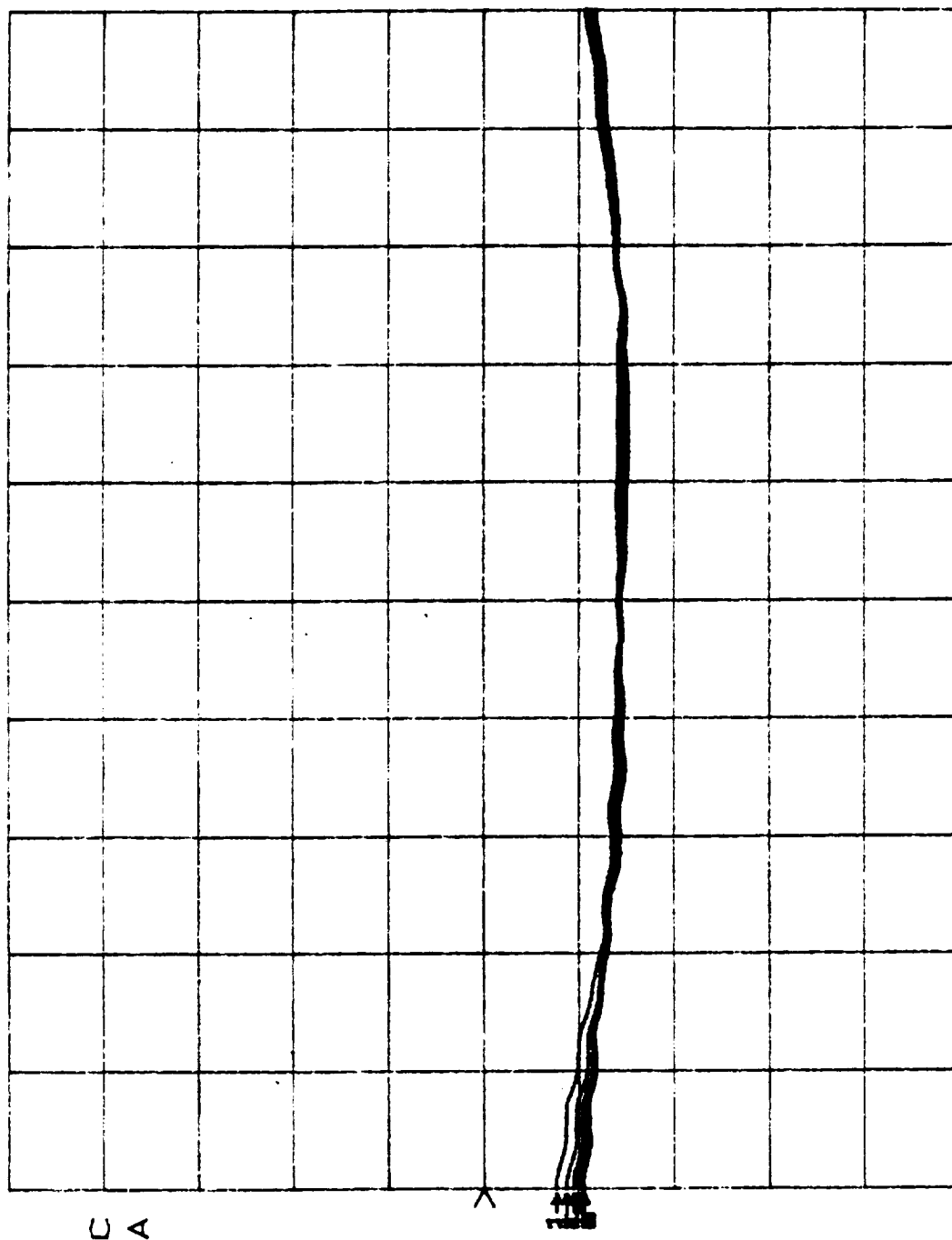
S22 log MAG
 REF 0.0 dB
 10.0 dB/



START 29.000000 1600 GHz
 STOP 31.500000 000 GHz

Figure A-14. Output Return Loss Versus Frequency for Unmodified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 13 States of Gain Control Amplifier).

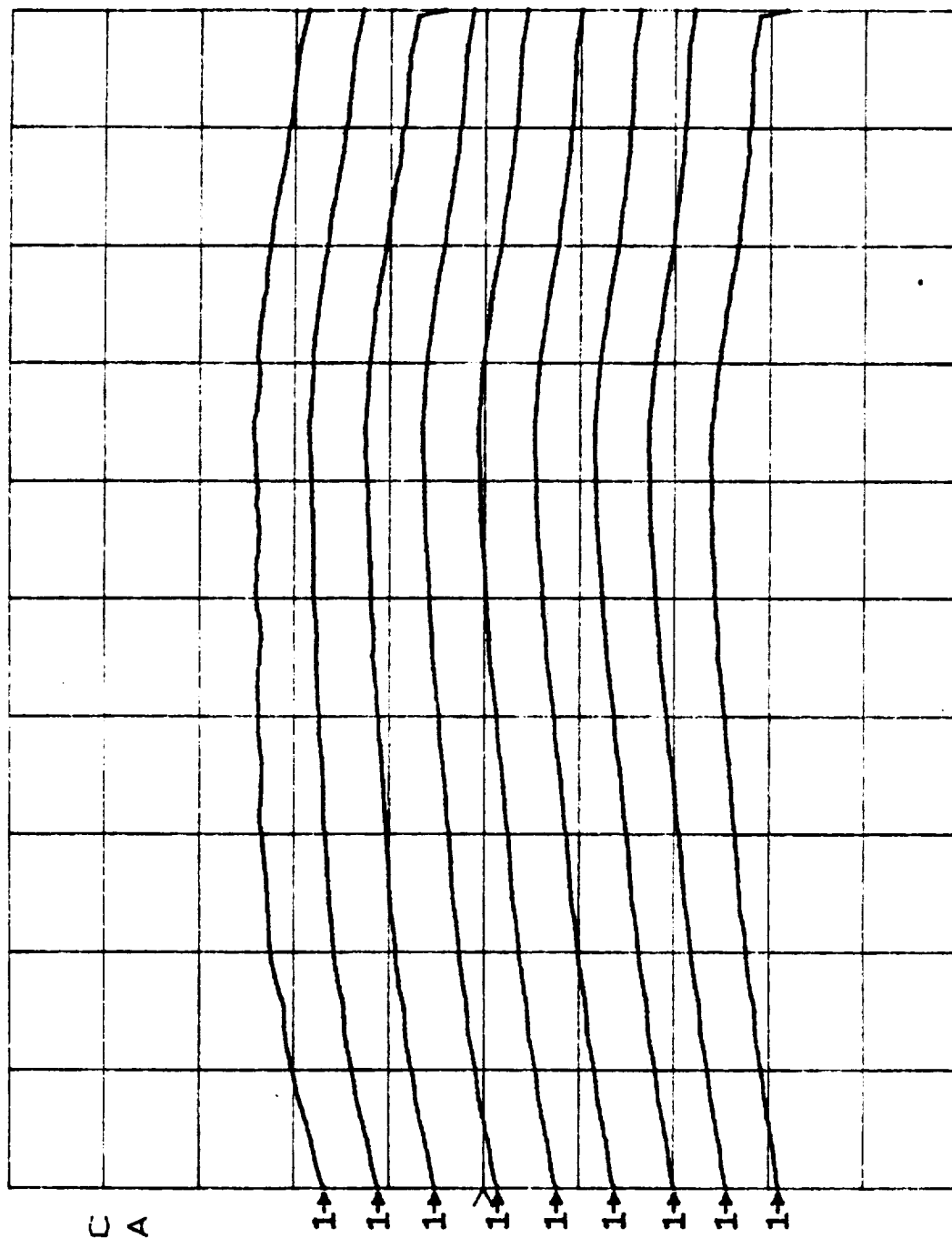
S11 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-15. Input Return Loss Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 9 States of Gain Control Amplifier).

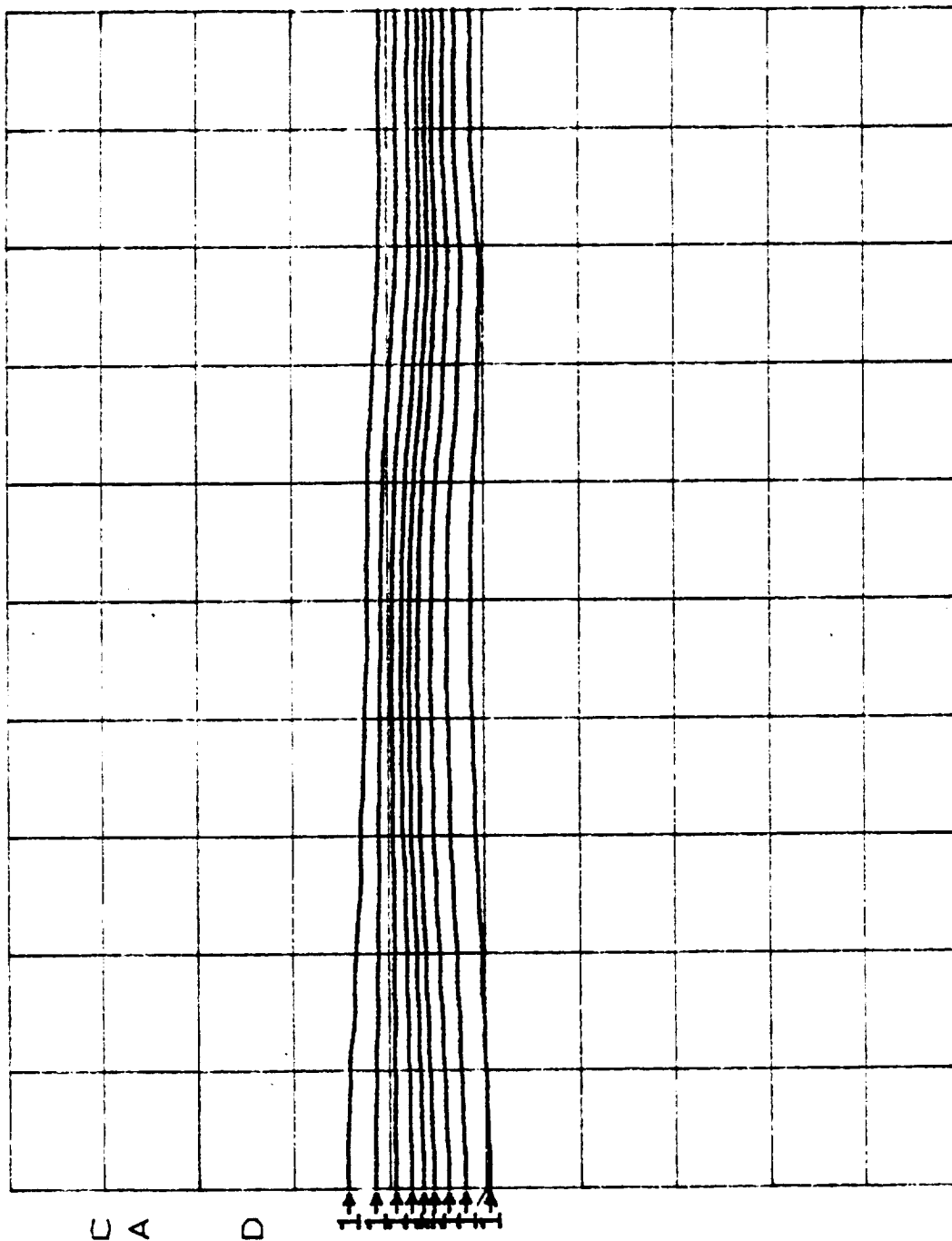
S21 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-16. Gain Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 9 States of Gain Control Amplifier).

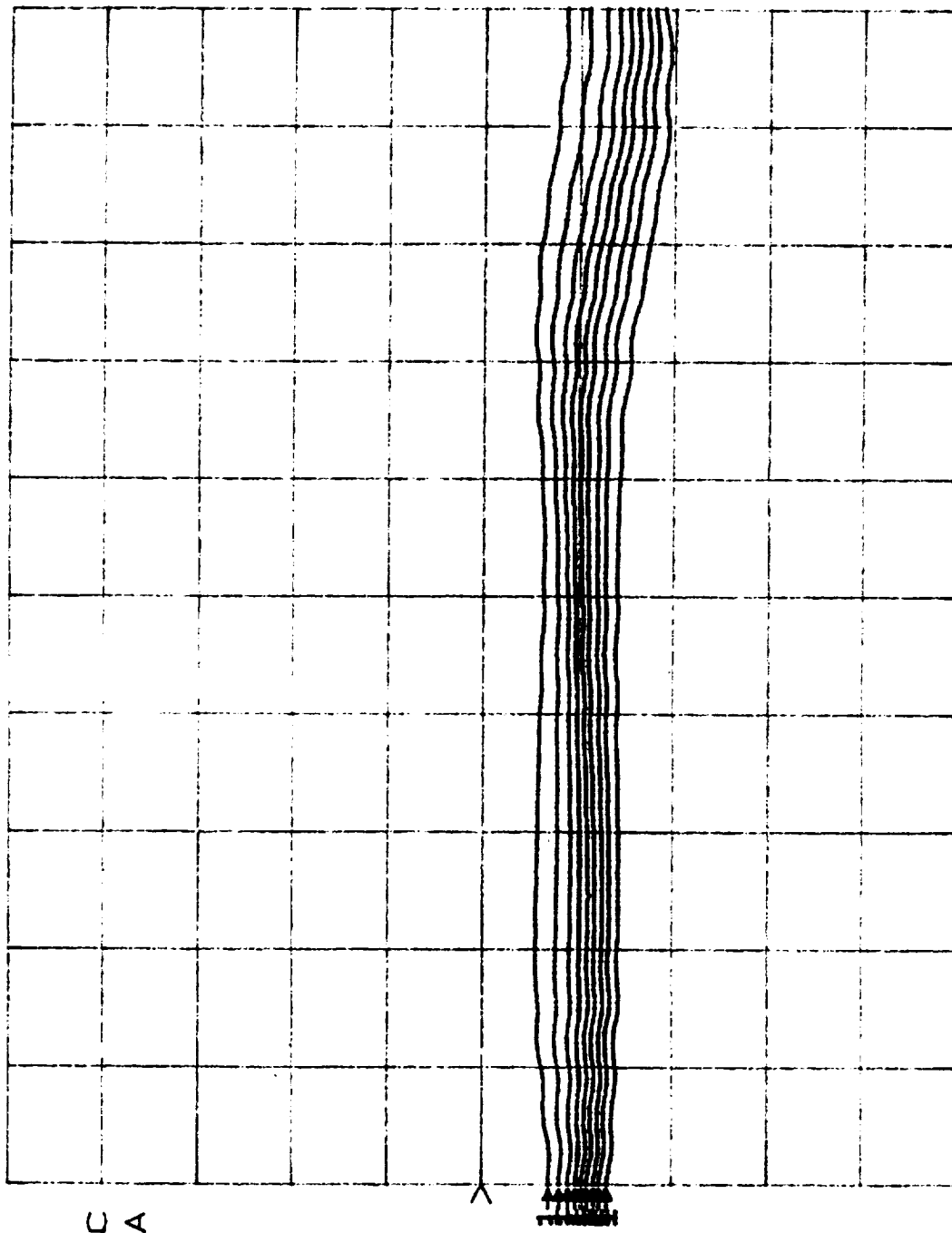
S21 \angle
 REF 0.0 °
 45.0 °/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-17. Insertion Phase Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 9 States of Gain Control Amplifier).

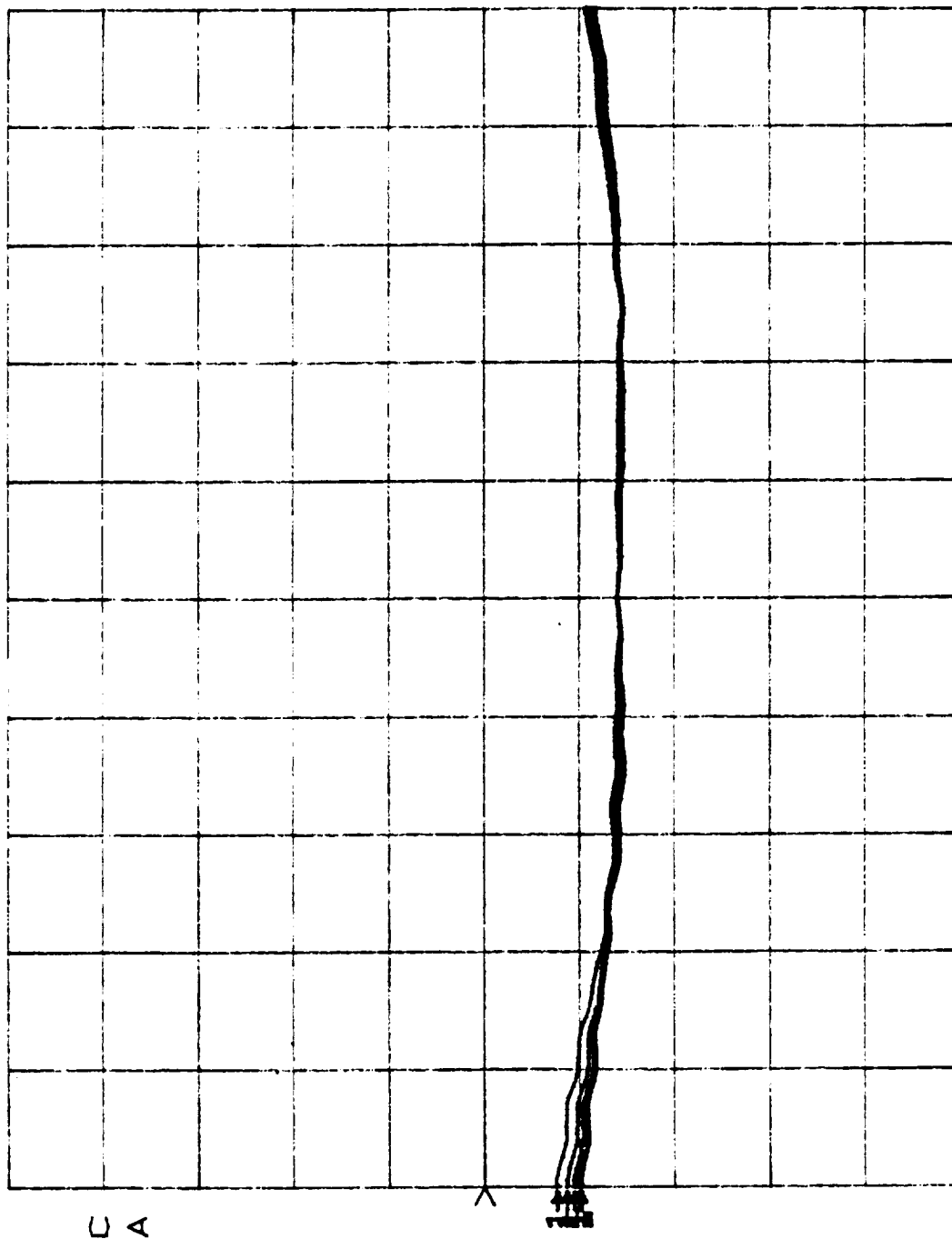
S22 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-18. Output Return Loss Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 9 States of Gain Control Amplifier).

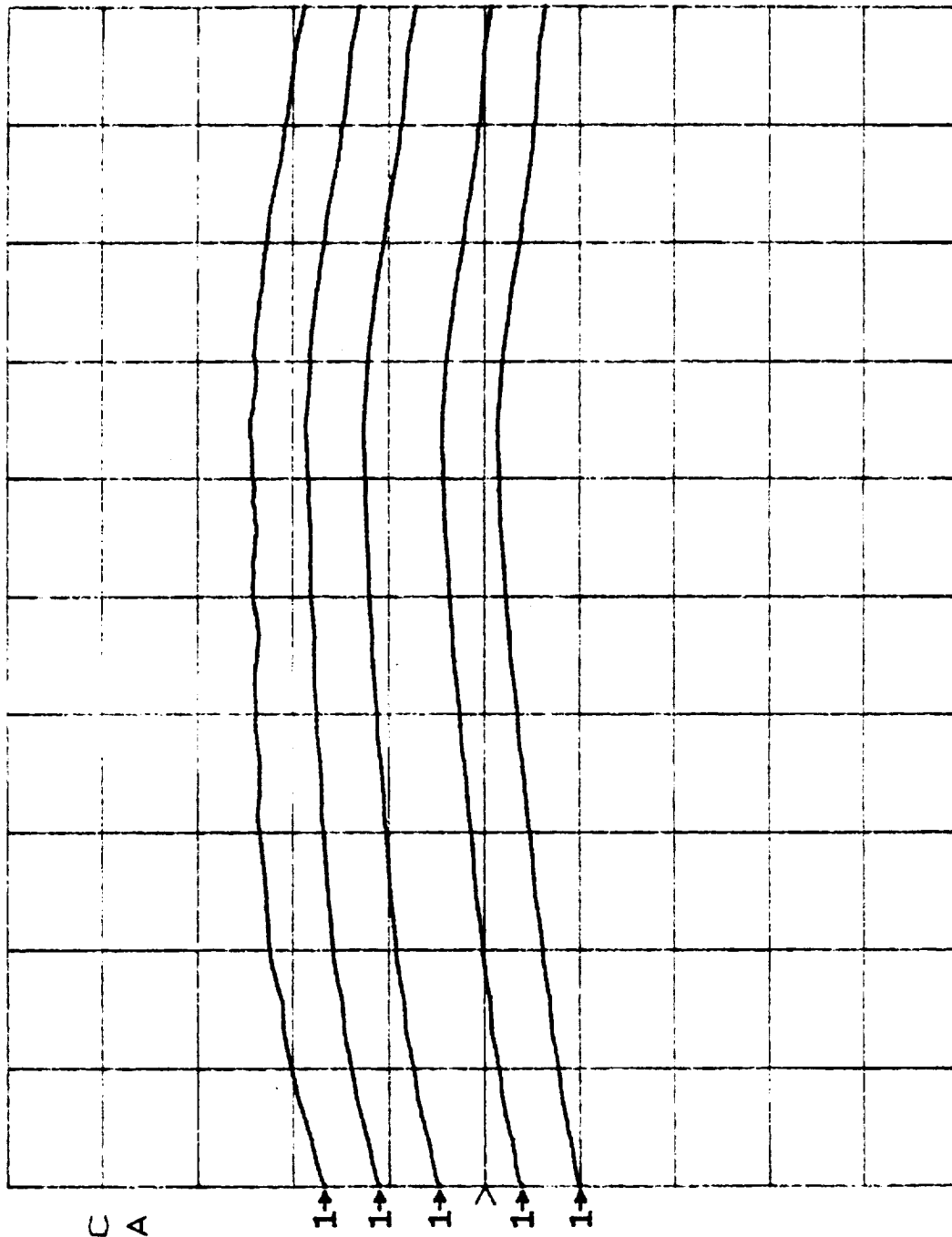
S11 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-19. Input Return Loss Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 5 States of Gain Control Amplifier).

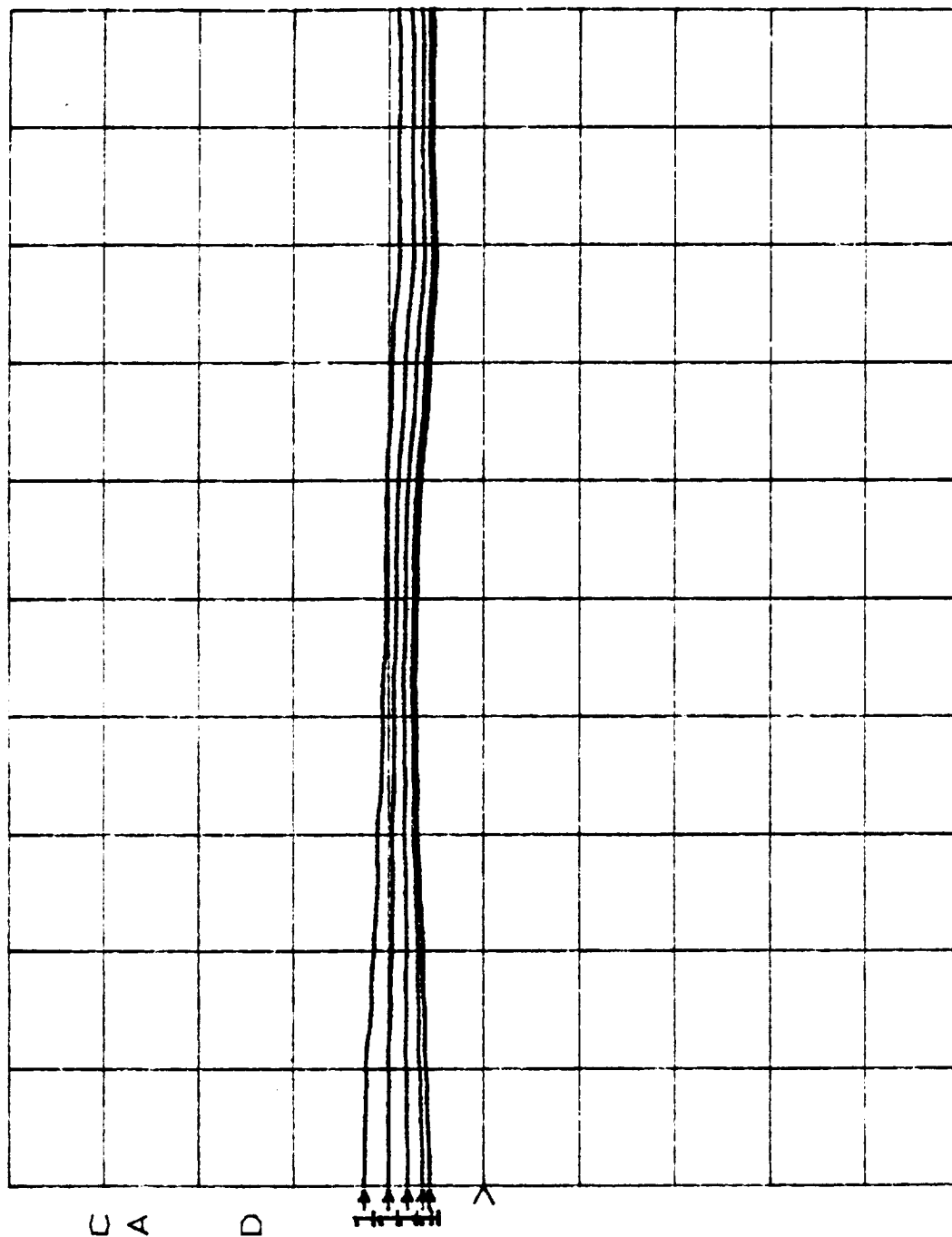
S21 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-20. Gain Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 5 States of Gain Control Amplifier).

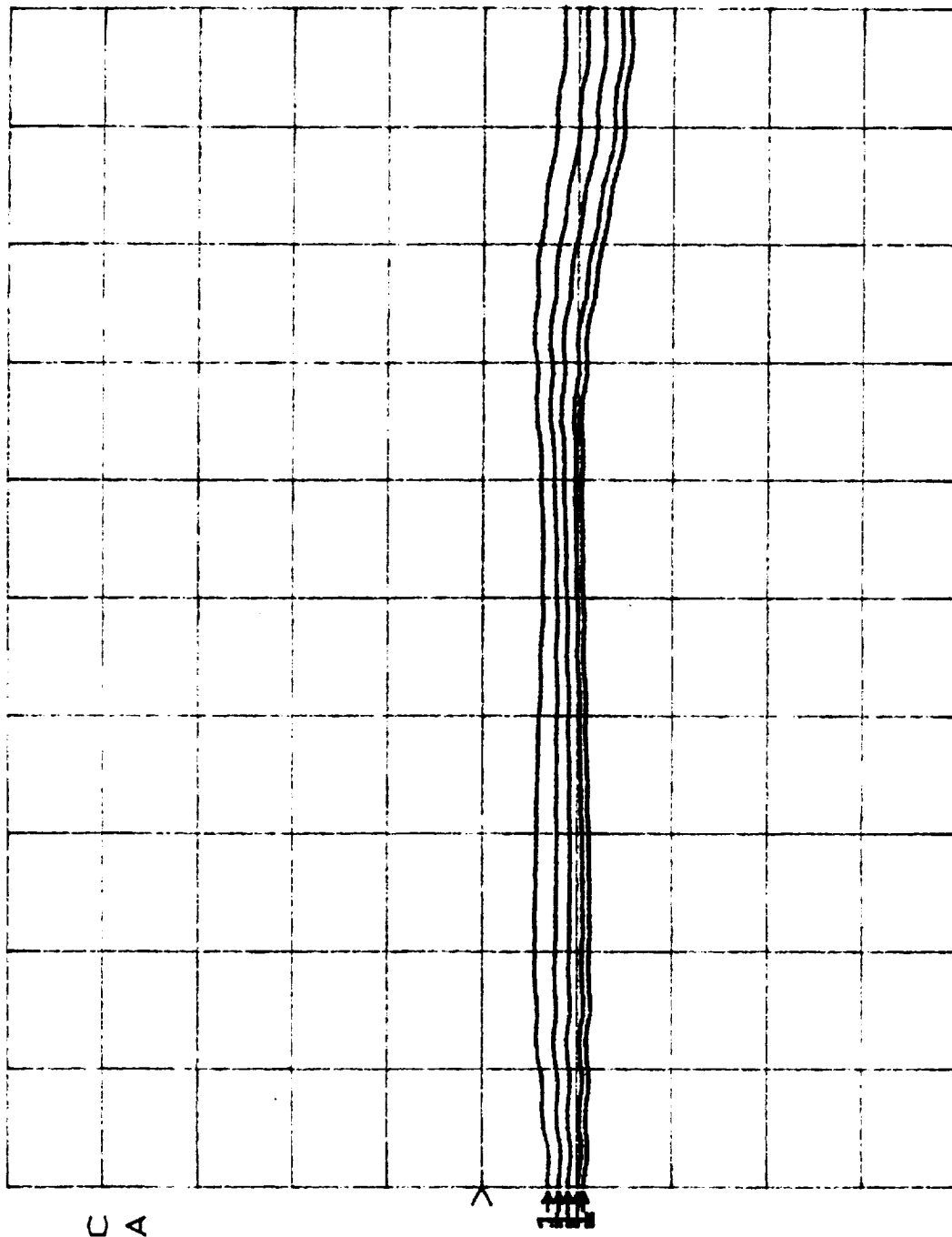
S21 \angle
 REF 0.0 °
 45.0 °/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-21. Insertion Phase Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 5 States of Gain Control Amplifier).

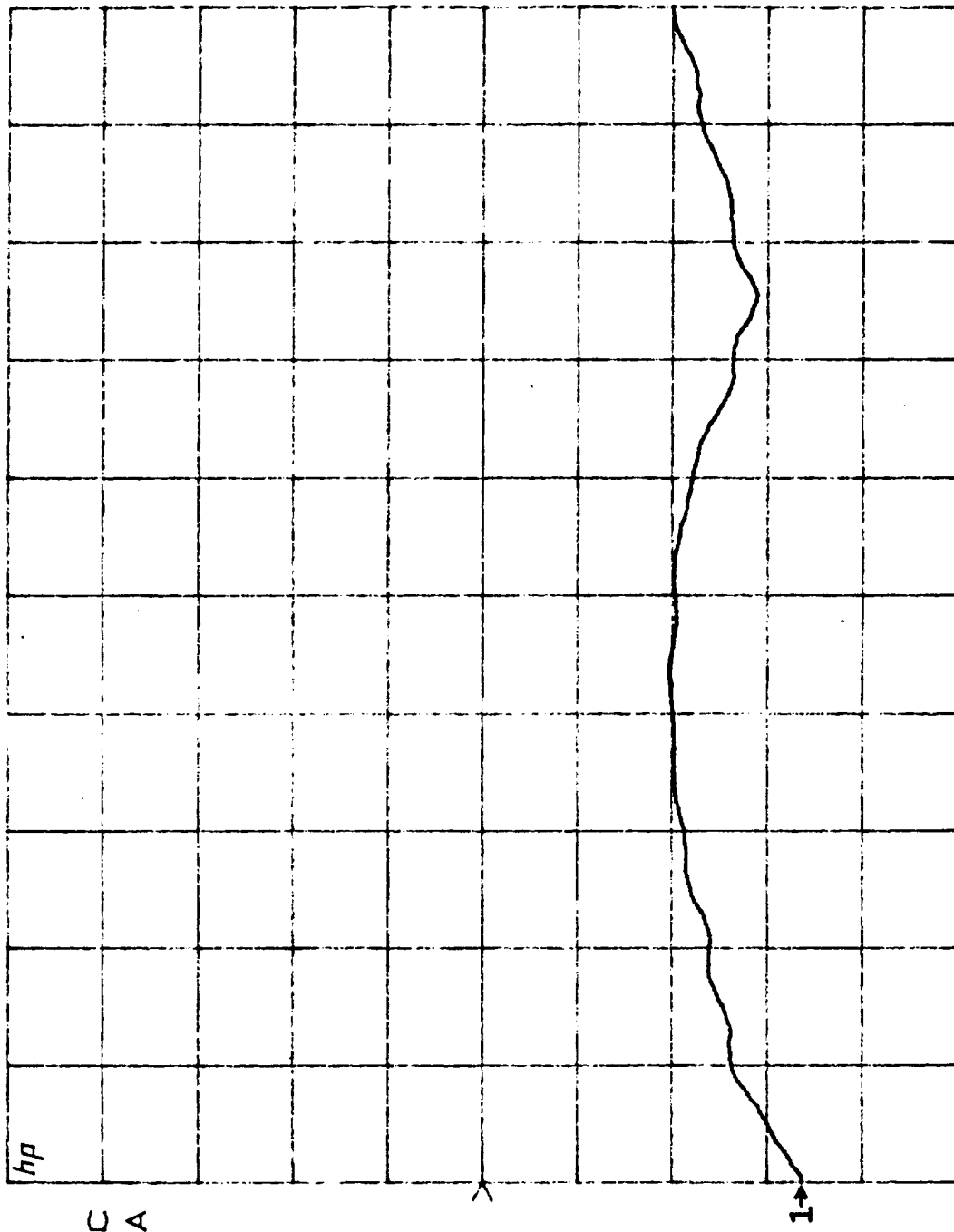
S22 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

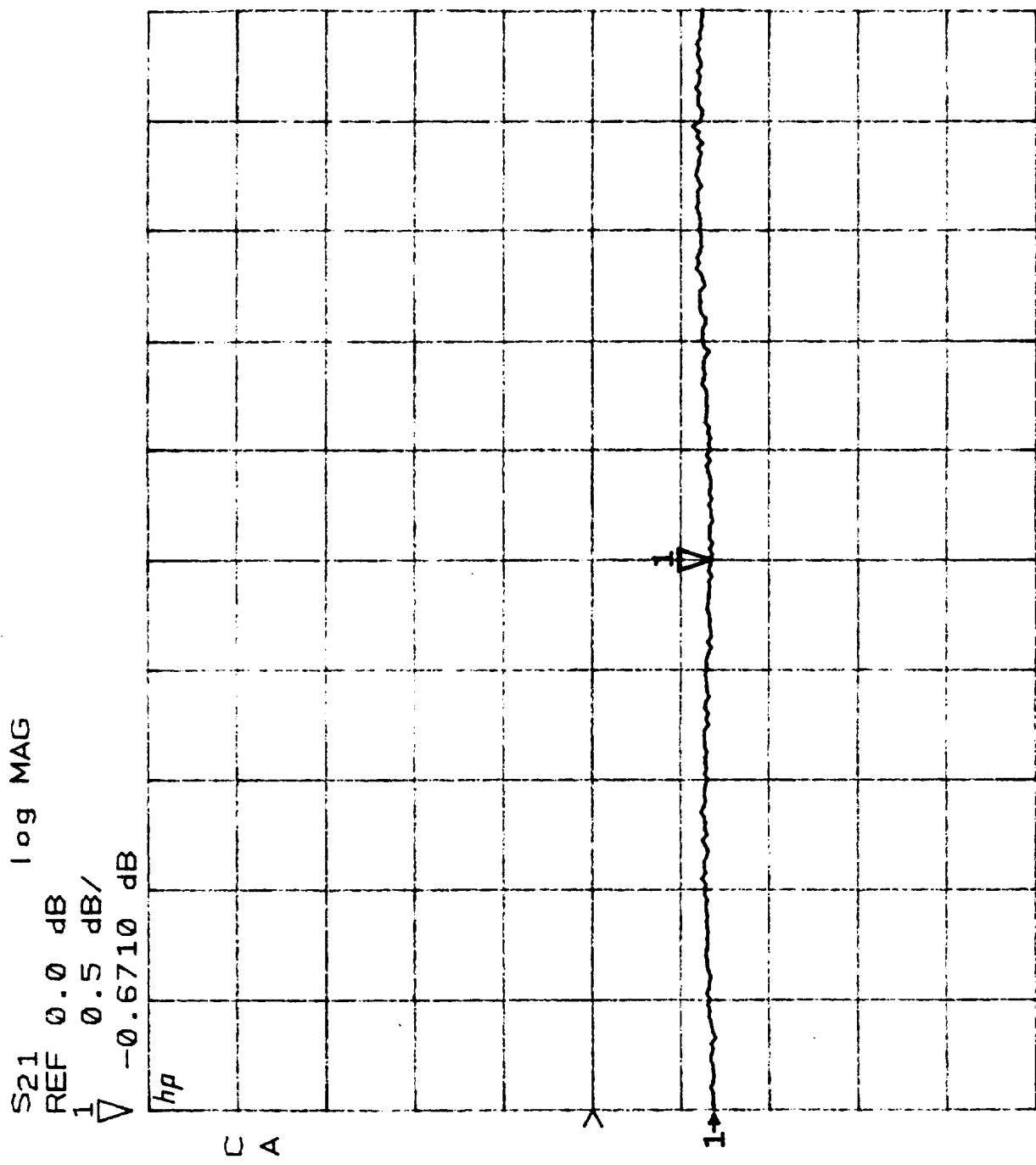
Figure A-22. Output Return Loss Versus Frequency for Modified Two-Stage Gain Control Amplifier from Wafer DG-85 (Superposition of 5 States of Gain Control Amplifier).

S_{11} log MAG
 REF 0.0 dB
 10.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure A-23. Input Return Loss Versus Frequency for Antipodal Fin-line Transition
 Used in the First Interconnected Receive Module.



START 27.500001600 GHz
 STOP 30.000000000 GHz
 Figure A-24. Insertion Loss Versus Frequency for Antipodal Fin-line Transition Used in the First Interconnected Receive Module.

APPENDIX B

INTERCONNECTED RECEIVE MODULE #1 DATA

GENERAL BIAS CONDITIONS FOR INTERCONNECTED RECEIVE MODULE #1

LOW NOISE AMPLIFIER:

Stage 1: $V_{GS} = -1.75 \text{ V}$
 $V_{DS} = 2.0 \text{ V}$
 $I_{DS} = 18.3 \text{ mA}$

Stage 2: $V_{GS} = -1.68 \text{ V}$
 $V_{DS} = 2.0 \text{ V}$
 $I_{DS} = 20.5 \text{ mA}$

PHASE SHIFTER:

Switched Line Bits: $V_{GS} = -5.5 \text{ V}$ or 0.0 V

Loaded Line Bit: $V_{GS} = -5.5 \text{ V (REF)}$
or
 $V_{GS} = -2.5 \text{ V (DELAY)}$

GAIN CONTROL AMPLIFIER:

Stage 1: $V_{GS} (1) = -0.88 \text{ V}$
 $V_{DS} = 2.9 \text{ V}$

Stage 2: $V_{GS} (1) = -0.76 \text{ V}$
 $V_{DS} = 3.4 \text{ V}$

GAIN SETTING	STAGE 1 AND 2 $V_{GS} (2)$	STAGE 1 I_{DS}	STAGE 2 I_{DS}
"12 dB"	-0.6 V	27.2 mA	29.5 mA
" 9 dB"	-0.74 V	26.0 mA	28.3 mA
" 6 dB"	-0.9 V	24.9 mA	27.1 mA
" 2 dB"	-1.15 V	22.9 mA	24.9 mA
"-1 dB"	-1.45 V	20.3 mA	22.2 mA

SPECIFIC BIAS CONDITIONS FOR FIGURES B-1 THRU B-8

- Figure B-1 Phase Shifter Switched Thru 4 States (0° , 90° , 180° , 270°) of Delay. Gain Control Amplifier Set at "6 dB" Gain State.
- Figure B-2 Phase Shifter in 0° Delay State. Gain Control Amplifier Switched Thru All 5 Gain States.
- Figure B-3 Phase Shifter in 0° Delay State. Gain Control Amplifier Switched Thru All 5 Gain States.
- Figure B-4 Phase Shifter Switched Thru 16 Delay States. Gain Control Amplifier Set at "6 dB" Gain State.
- Figure B-5 Phase Shifter Switched Thru 16 Delay States. Gain Control Amplifier Set at "6 dB" Gain State.
- Figure B-6 Phase Shifter in 0° Delay State. Gain Control Amplifier Switched Thru All 5 Gain States.
- Figure B-7 Phase Shifter Switched Thru 4 States (0° , 22° , 45° , 67°) of Delay. Gain Control Amplifier Set at "6 dB" Gain State.
- Figure B-8 Phase Shifter in 0° Delay State. Gain Control Amplifier Switched Thru All 5 Gain States.

FIGURE CAPTIONS FOR APPENDIX B

- Figure B-1 Input Return Loss Versus Frequency for Interconnected Receive Module #1 (Superposition of 4 States of Phase Shifter with Low Noise Amplifier and Gain Control Amplifier Fixed).
- Figure B-2 Gain Versus Frequency for Interconnected Receive Module #1 (Superposition of 5 States of Gain Control Amplifier with Low Noise Amplifier and Phase Shifter Fixed).
- Figure B-3 Insertion Phase Versus Frequency for Interconnected Receive Module #1 (Superposition of 5 States of Gain Control Amplifier with Low Noise Amplifier and Phase Shifter Fixed).
- Figure B-4 Gain Versus Frequency for Interconnected Receive Module #1 (Superposition of 16 States of Phase Shifter with Low Noise Amplifier and Gain Control Amplifier Fixed).
- Figure B-5 Insertion Phase Versus Frequency for Interconnected Receive Module #1 (Superposition of 16 States of Phase Shifter with Low Noise Amplifier and Gain Control Amplifier Fixed).
- Figure B-6 Output Return Loss Versus Frequency for Interconnected Receive Module #1 (Superposition of 5 States of Gain Control Amplifier with Phase Shifter and Low Noise Amplifier Fixed).
- Figure B-7 Output Return Loss Versus Frequency for Interconnected Receive Module #1 (Superposition of 4 States of Phase Shifter with Low Noise Amplifier and Gain Control Amplifier Fixed).

Figure B-8 Reverse Isolation Versus Frequency for Interconnected Receive Module #1 (Superposition of 5 States of Gain Control Amplifier with Low Noise Amplifier and Phase Shifter Fixed).

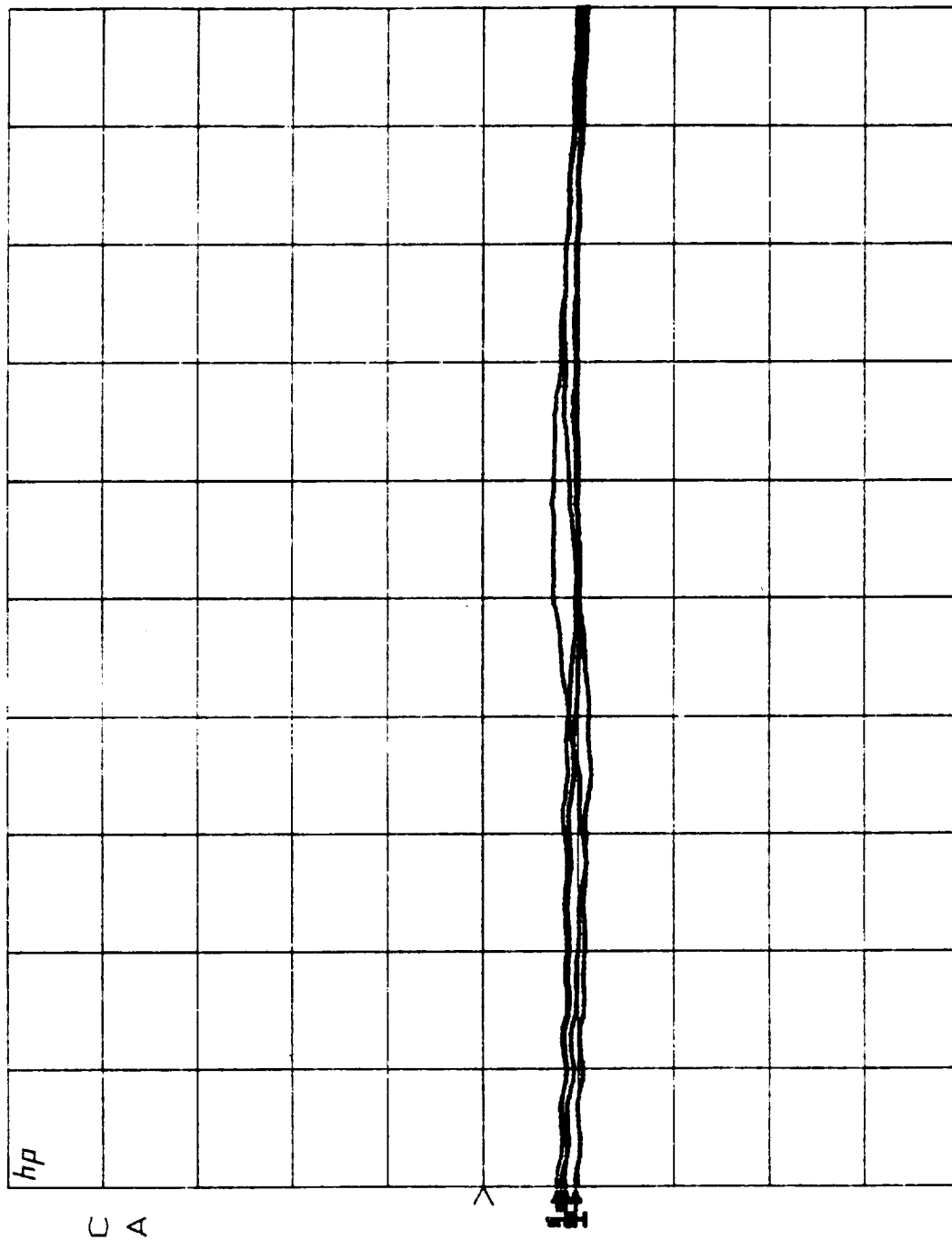
NOISE FIGURE DATA FOR INTERCONNECTED RECEIVE MODULE #1

$f = 28.75 \text{ GHz}$

GAIN SETTING	NOISE FIGURE
"12 dB"	14.0 dB
" 9 dB"	14.8 dB
" 6 dB"	15.7 dB
" 2 dB"	17.2 dB
"-1 dB"	18.5 dB

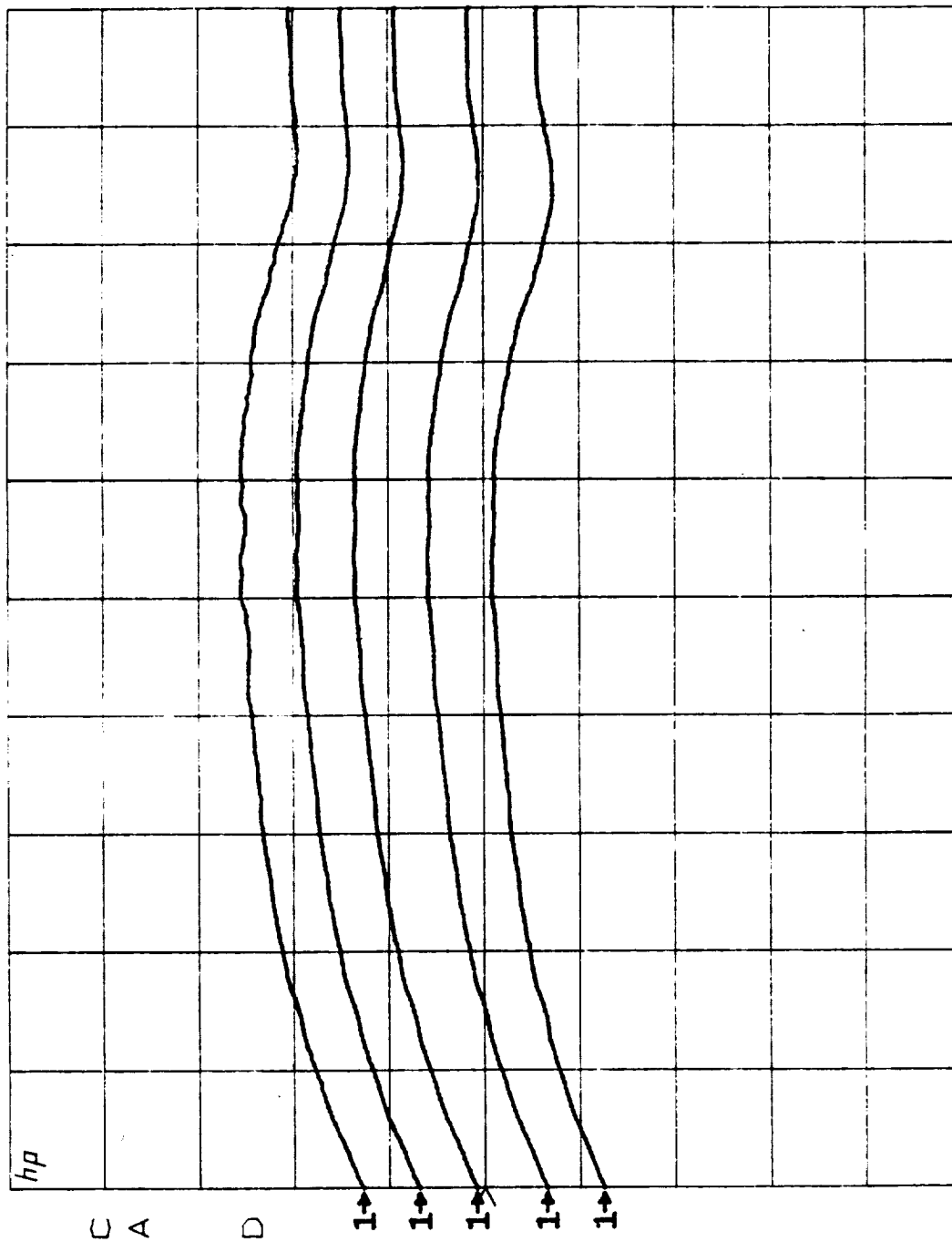
Phase Shifter Set at 0° Delay.

S11 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz
 Figure B-1. Input Return Loss Versus Frequency for Interconnected Receive Module #1
 (Superposition of 4 States of Phase Shifter with Low Noise Amplifier and
 Gain Control Amplifier Fixed).

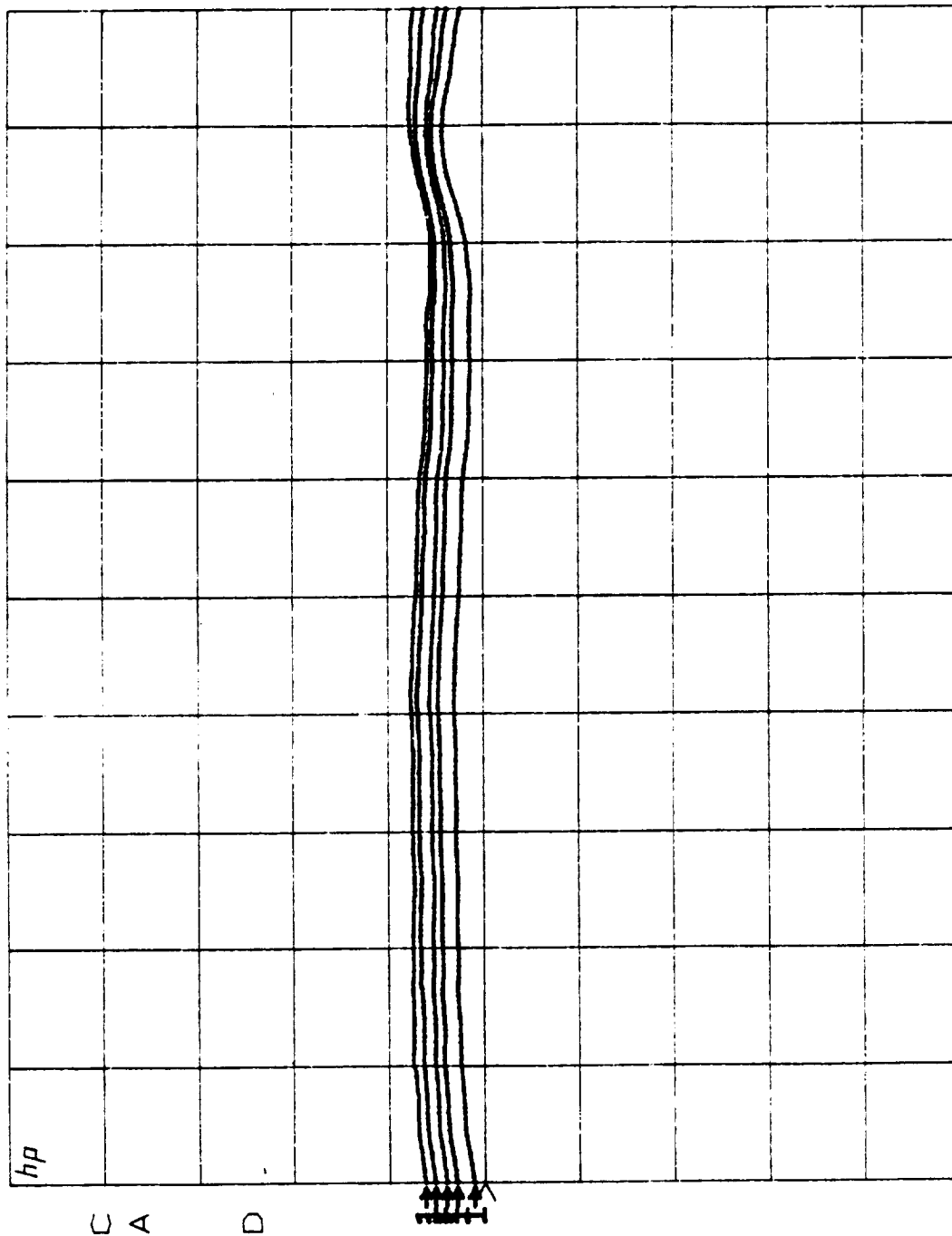
S21 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

Figure B-2. Gain Versus Frequency for Interconnected Receive Module #1 (Superposition of 5 States of Gain Control Amplifier with Low Noise Amplifier and Phase Shifter Fixed).

S21 \angle
 REF 0.0 °
 45.0 °/



START 27.500001600 GHz
 STOP 30.000000000 GHz
 Figure B-3. Insertion Phase Versus Frequency for Interconnected Receive Module #1
 (Superposition of 5 States of Gain Control Amplifier with Low Noise
 Amplifier and Phase Shifter Fixed).

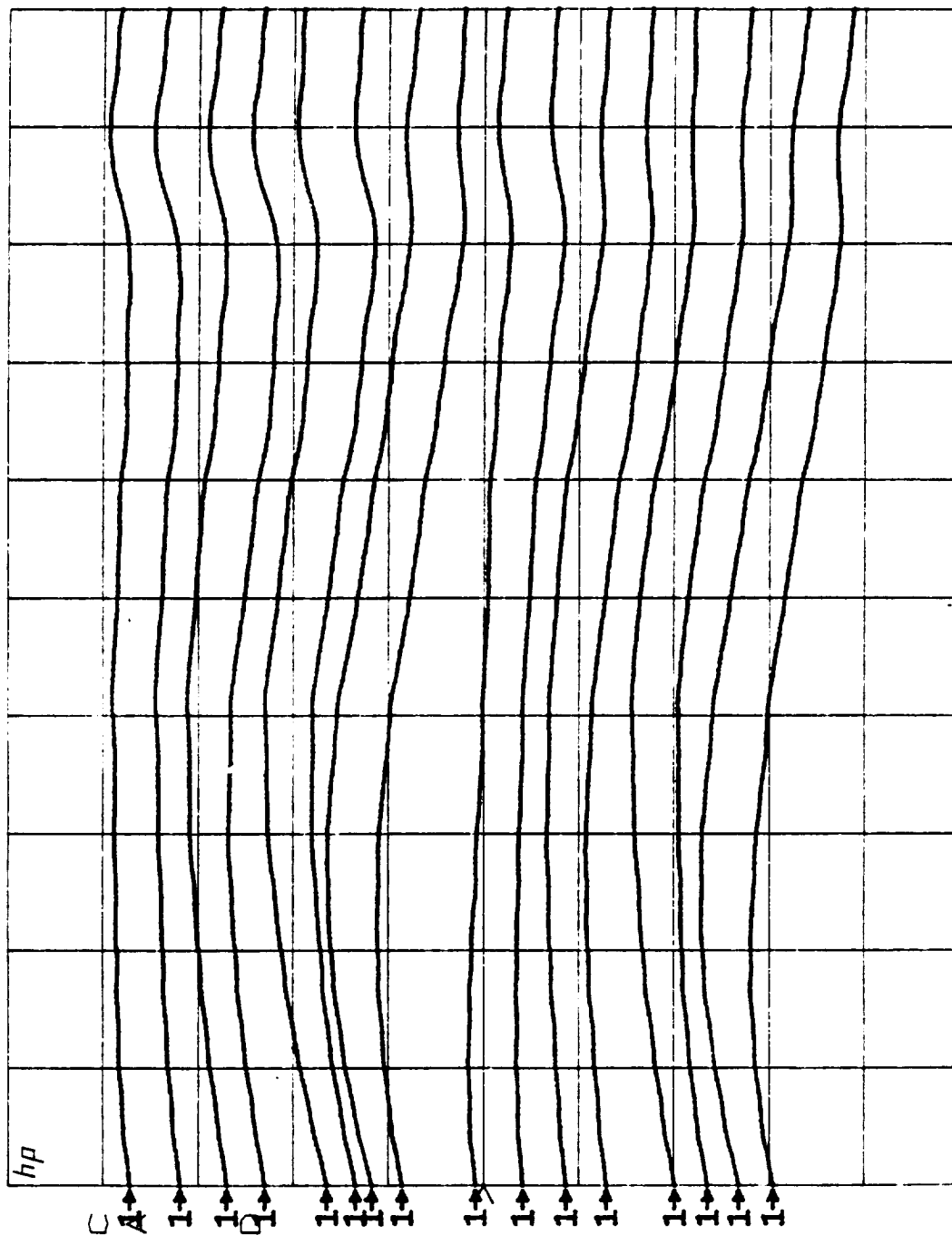
S21 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001600 GHz
 STOP 30.000000000 GHz

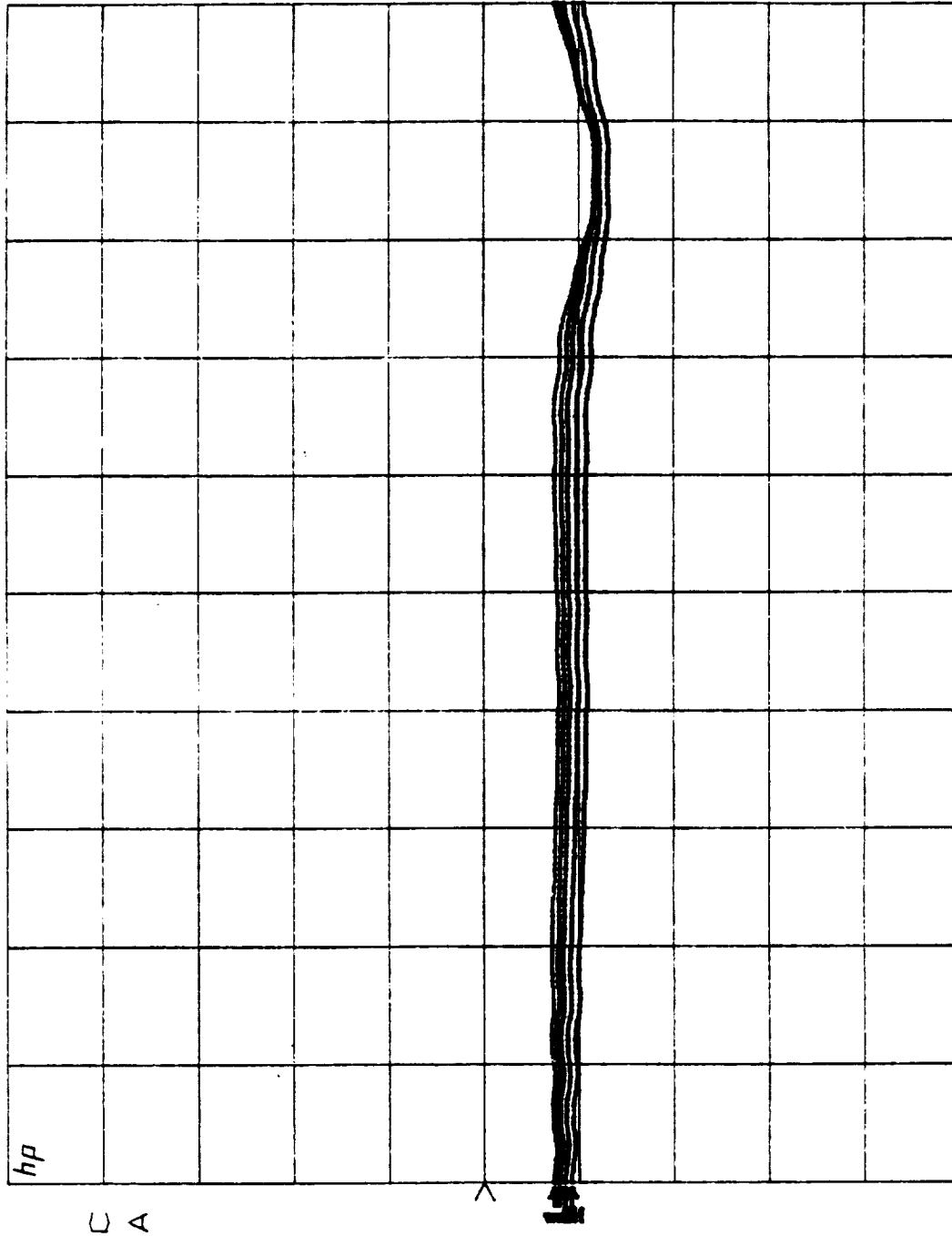
Figure B-4. Gain Versus Frequency for Interconnected Receive Module #1 (Superposition of 16 States of Phase Shifter with Low Noise Amplifier and Gain Control Amplifier Fixed).

S_{21} \angle
 REF 0.0 °
 45.0 °/



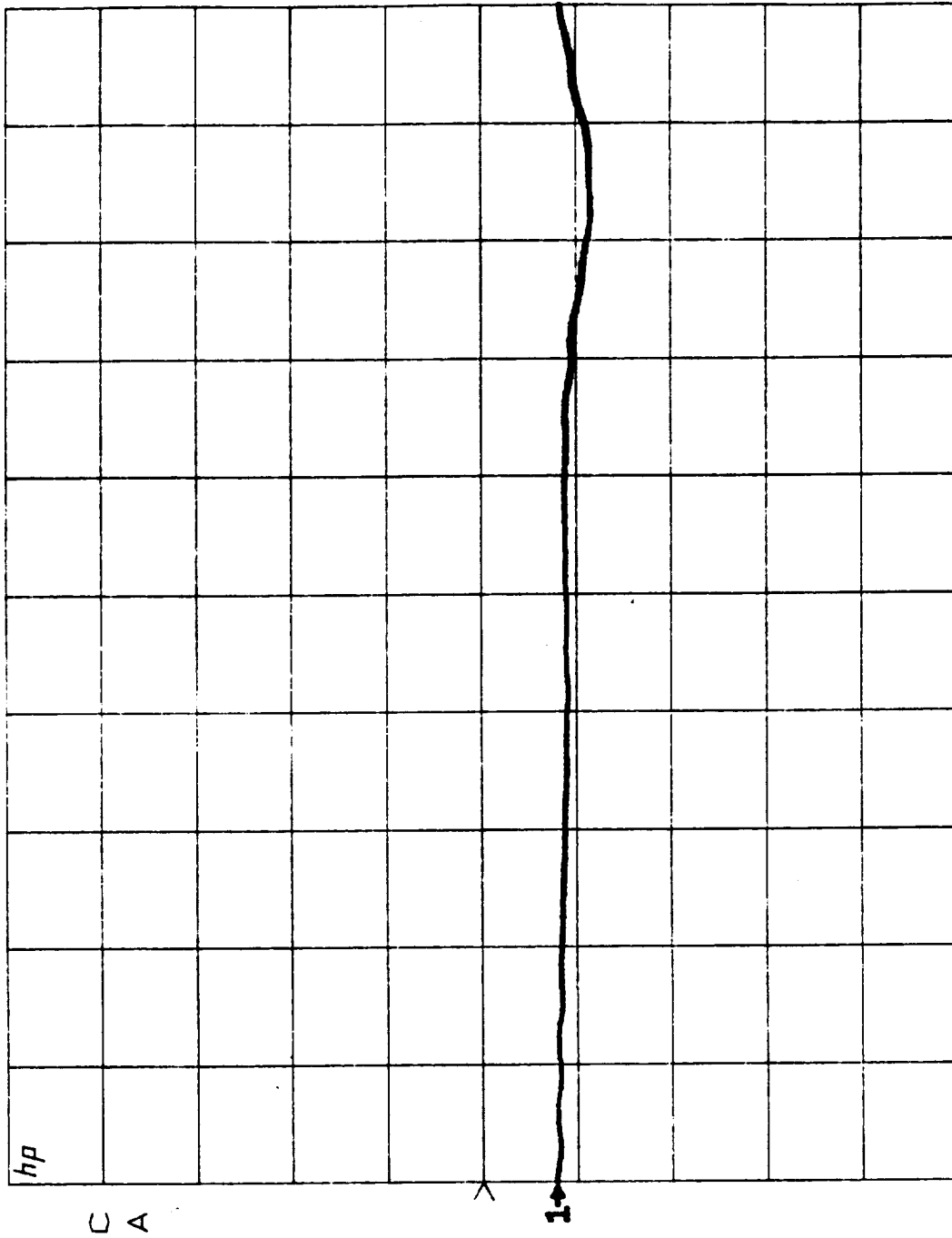
START 27.500001600 GHz
 STOP 30.000000000 GHz
 Figure B-5. Insertion Phase Versus Frequency for Interconnected Receive Module #1
 (Superposition of 16 States of Phase Shifter with Low Noise Amplifier
 and Gain Control Amplifier Fixed).

S22 log MAG
 REF 0.0 dB
 5.0 dB/



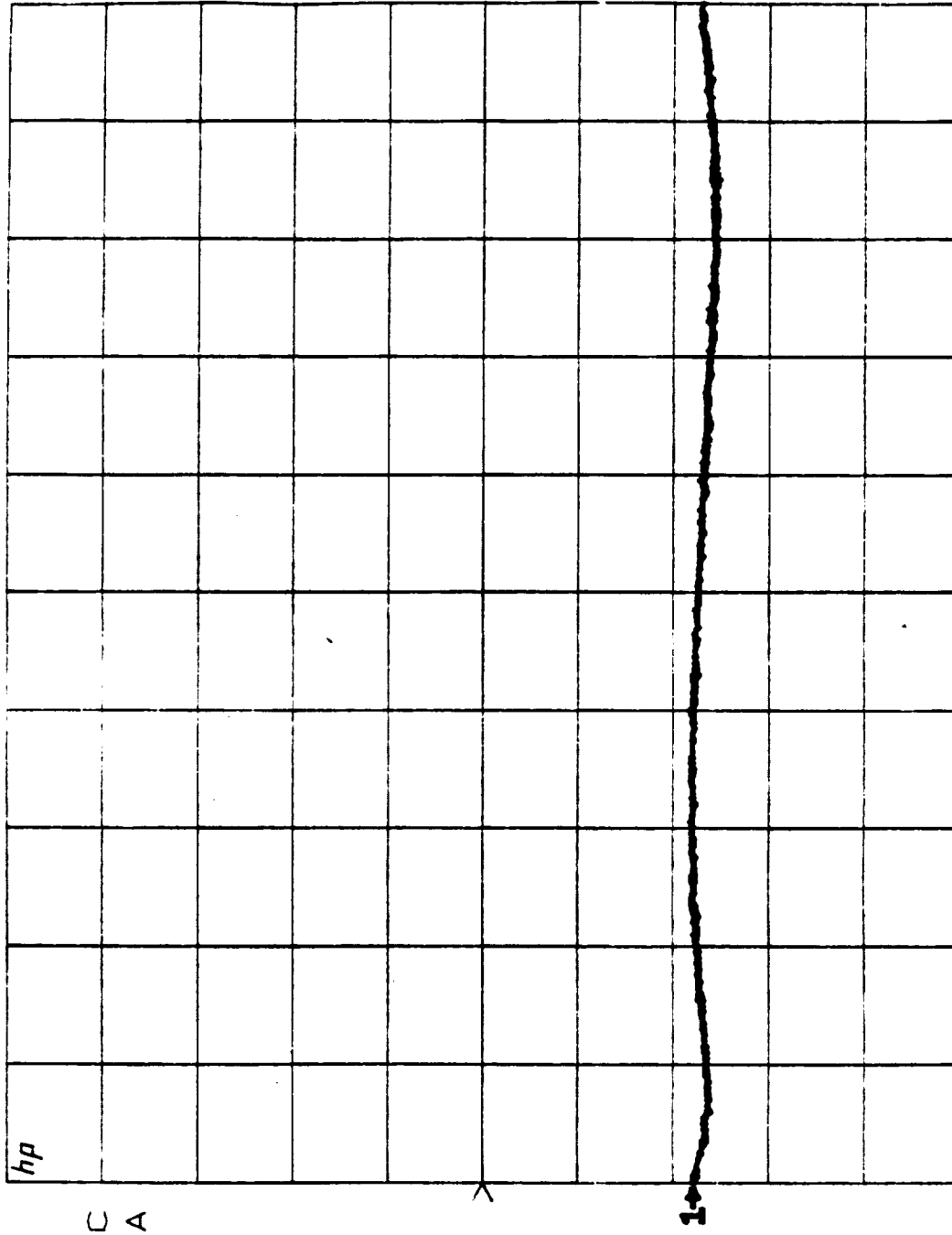
START 27.500001000 GHz
 STOP 29.999999400 GHz
 Figure B-6. Output Return Loss Versus Frequency for Interconnected Receive Module #1
 (Superposition of 5 States of Gain Control Amplifier with Phase Shifter
 and Low Noise Amplifier Fixed).

S22 log MAG
 REF 0.0 dB
 5.0 dB/



START 27.500001000 GHz
 STOP 29.999999400 GHz
 Figure B-7. Output Return Loss Versus Frequency for Interconnected Receive Module #1
 (Superposition of 4 States of Phase Shifter with Low Noise Amplifier
 and Gain Control Amplifier Fixed).

S12 log MAG
 REF 0.0 dB
 20.0 dB/



START 27.500001000 GHz
 STOP 29.99999400 GHz

Figure B-8. Reverse Isolation Versus Frequency for Interconnected Receive Module #1
 (Superposition of 5 States of Gain Control Amplifier with Low Noise Amplifier and Phase Shifter Fixed).

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